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Non-Ideal Push–Pull Converter Model: Trade-Off between Complexity and Practical Feasibility in Terms of Topology, Power and Operating Frequency

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Abstract: Power converters are the basic elements of any power electronics system in many areas and applications. Among them, the push–pull converter topology is one of the most widespread due to its high efficiency, versatility, galvanic isolation, reduced number of switching devices and the possibility of implementing high conversion ratios with respect to non-isolated topologies. Optimal design and control requires very accurate models that consider all the non-idealities associated with the actual converter. However, this leads to the use of high-order models, which are impractical for the design of model-based controllers in real-time applications. To obtain a trade-off model that combines the criteria of simplicity and accuracy, it is appropriate to assess whether it is necessary to consider all non-idealities to accurately model the dynamic response of the converter. For this purpose, this paper proposes a methodology based on a sensitivity analysis that allows quantifying the impact of each non-ideality on the converter behaviour response as a function of the converter topology, power and frequency. As a result of the study, practical models that combine the trade-off between precision and simplicity are obtained. The behaviour of the simplified models for each topology was evaluated and validated by simulation against the most complete and accurate non-ideal model found in the literature. The results have been excellent, with an error rate of less than 5% in all cases.

Keywords: DC–DC power converter; isolated DC–DC; push–pull converter; modelling; non-ideal model

Citation: Vivas, F.J.; Andújar, J.M.; Segura, F. Non-Ideal Push–Pull Converter Model: Trade-Off between Complexity and Practical Feasibility in Terms of Topology, Power and Operating Frequency. *Appl. Sci.* **2024**, *14*, 6224. https://doi.org/10.3390/app14146224

Academic Editors: Gerard Ghibaudo, Pedro Eduardo Melín Coloma, Eduardo Espinosa Neira and Ricardo Lizana Fuentes

Received: 20 May 2024
Revised: 29 June 2024
Accepted: 16 July 2024
Published: 17 July 2024

1. Introduction

DC–DC power converters, in their isolated and non-isolated variants, are a fundamental part of the design of switch-mode power supplies (SMPS) [1]. Among all possible converter configurations, the push–pull topology is one of the most widely used architectures in power electronics design (SMPS and power inverters) [2]. There are many advantages of this architecture compared to other converter topologies: with respect to non-isolated topologies, its high input–output ratio and galvanic isolation [2]; with respect to isolated topologies in general, the reduced number of switching devices and, consequently, the associated lower losses; with respect to half-bridge and full-bridge topologies in particular, the lower complexity for their control (the sink of the power transistors is referenced to the circuit ground); and, finally, with respect to single-switch topologies, its high efficiency and the excellent utilisation of the high-frequency transformer [3]. Moreover, these particular characteristics confer a wide range of operating powers, varying from a few watts to tens of kW, with typical switching frequencies between 20 kHz and 500 kHz, depending on size, cost and performance constraints [4].

Thanks to all of the above advantages, the range of applications of this topology is becoming more and more diverse. Some of the most significant and recent examples of the use of push–pull topology are electric propulsion systems in electric vehicles [5], the integration of renewable energy sources in microgrids [6] and the integration of energy

storage systems based on supercapacitors [7], batteries [8] or hydrogen technologies [9]. This is the reason for the special interest in the study of this topology.

For their implementation and the design of model-based controllers in real applications, it is essential to have analytical models as representative as possible of the real behaviour of the converter [10]. For this purpose, it is crucial that the push–pull converter model considers its intrinsic non-idealities, or at least those representatives in real applications, which may vary depending on the converter topology and the rated power and operating frequency [10]. Determining the correct model must be a trade-off between accuracy and simplicity, which is not always an easy task. To this end, the search for trade-off solutions must consider that an overly complex model increases its computational burden for the implementation of real-time controllers. However, a high simplification may generate a large deviation between the proposed model and the real converter, which will have a negative impact on the performance and behaviour of the converter–controller duo [10]. Therefore, it is necessary to analyse on a case-by-case basis the possible influence that certain non-idealities may have on the dynamic and steady-state response of the converter depending on the application and operating conditions.

Many papers in the scientific literature propose and validate push–pull converter models for different uses and applications. Although all of them start from the ideal model of the converter (Figure 1), the main difference between the different variants lies in the non-idealities considered for their definition.

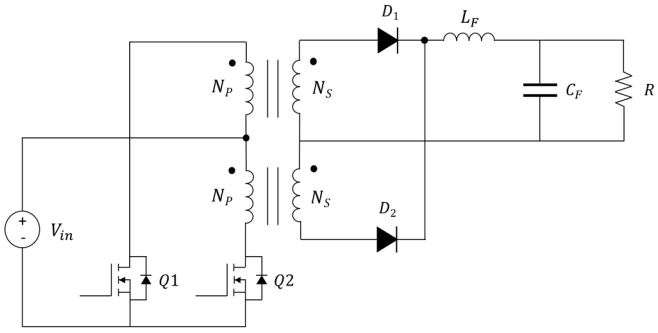

Figure 1. Ideal electrical circuit of the push–pull converter.

First, the most widespread solutions are based on the complete ideal model of the converter (Figure 1). This model is based on the analysis of the second-order buck equivalent model of the transformer secondary circuit and has been successfully applied in the scientific literature in different applications and scales, among others, for the management and power supply to LED lighting systems [11]; the control and management of renewable energy sources, wind and photovoltaic, in microgrids [12,13]; the integration of energy storage systems based on hydrogen technologies in HVDC buses [9] and the design of charge balancing circuits in battery management systems [14], as well as in the design of battery chargers for electric vehicles applications [15,16]. Although this model can provide in certain cases an acceptable behaviour for the sizing and design of control loops, the performance obtained in real systems, depending on the topology and operating conditions, can present large discrepancies when non-idealities of the converter components are neglected [17].

Among other applications, non-idealities related to transformer winding resistances are considered in the design of DC/DC converters for the implementation of MPPT algorithms in PV applications [18]. Similarly, non-idealities associated with the LC output filter are considered for the design and control of inverters for stand-alone PV applications [19]. Since the non-idealities associated with energy storage elements (coils or capacitors) are not included, these models are designed and have the same order and dynamic characteristics as the ideal model.

Simplified and also reduced-order models are found for the design and control of photovoltaic generation systems [20,21], the design and control of electric vehicle power

train inverters [5] and the development of soft-switching techniques [22,23], in which only the transformer leakage inductances are modelled.

In turn, models integrating the non-idealities of power switching devices have been developed for the design and control of three-phase inverters [24]. More complex models, in which non-idealities related to transformer windings are also modelled, have been formulated for the control of fuel cell-based power supplies [25], as well as for the charge and discharge management of supercapacitor modules [7].

Finally, more complete and complex models that consider the full non-ideal transformer model and the effect of the output capacitance of power switching devices are used for the design and control of auxiliary power systems with HVDC buses for use in stand-alone applications [26], medium-power DC applications [27], as well as the design and control of fuel cell-based power systems [28].

The inclusion of the above non-idealities allows these models to better approximate the dynamic response of the real converter at the cost of increasing the order of the model. The order, complexity and accuracy of each model will depend a priori on the number of non-idealities considered, as well as the type of topology, power and operating frequency.

From a review of the scientific literature, none of the reviewed works justifies the choice of the proposed model and therefore the choice of whether to include non-idealities based on their effect on its dynamic response. Therefore, given the lack of criteria, it cannot be affirmed that the model used in each work is the most appropriate.

To overcome the deficiencies found in the scientific literature, where there are no works in which a complete analysis as the one proposed here is carried out, the research developed in this work allows obtaining the best equivalent control-oriented model that meets the right balance between simplicity and accuracy. For this purpose, this work presents a design methodology based on the results obtained from a very complete sensitivity analysis for the identification of the influence of the different non-idealities associated with real converters considering different topologies and operating conditions, starting from the complete non-ideal model of the converter previously developed by the authors in [17].

Thus, the main contributions of this work can be summarised as follows:

- The definition of a methodology based on the development of a sensitivity analysis that allows to identify the impact and the role that each non-ideality of the converter has on the dynamic and steady-state response of its equivalent model;
- The sensitivity analysis performed allows the identification, proposal and validation of non-ideal models oriented to the control of push–pull converters, considering the trade-off between accuracy and practical application;
- The establishment of cause–effect relationships for each of the non-idealities of the converter with respect to their influence on the accuracy of the model, depending on the converter topology and its operating conditions;
- The identification, proposal and validation of non-ideal committed control-oriented circuits and models for the push–pull converter that combine precision and simplicity (reduced order) based on the proposed methodology and sensitivity analysis;
- Both buck and boost topologies have been analysed under real operating conditions of push–pull converters.

Based on the above, the conclusions obtained from this work will allow the development of digital twins, as well as the realisation of advanced studies and model-based control techniques.

The remainder of this paper is organised as follows: Section 2 studies the operating modes of the converter and presents its complete non-ideal equivalent circuit and complete model. Section 3 presents a methodology for the sizing and estimation of the main parameters associated with the non-ideal model of the converter, necessary to perform the study and sensitivity analysis developed in Section 4. In this section, the influence of the non-idealities on the converter behaviour is analysed for the two topologies and four practical case studies. Section 5 presents the conclusions derived from the sensitivity analysis for the identification, design and subsequent validation of the trade-off models

between complexity and feasibility. Finally, Section 6 concludes the paper and presents future works to be undertaken.

2. Push–Pull Converter: Operating Principle and Non-Ideal Electrical Model

This section describes the operating principle of the push–pull converter and presents its equivalent circuit together with the main non-idealities that determine its equivalent model.

2.1. Push–Pull Converter Operating Principle

The operation of the push–pull converter is determined by the controlled flow of current in the primary transformer circuit and by magnetic induction in the secondary circuit. This control is accomplished by controlled operation of the power switching devices and energy storage in the inductor and capacitor of the output low-pass filter (L_F-C_F). The electrical schematic of the ideal circuit is shown in Figure 1. In [17] a half-bridge rectifier topology was chosen for the converter output stage (which will be logically maintained in this study), as it reduces the number of semiconductors and their associated losses (which can be considerable especially in high-power buck topologies operating at high output currents) while simplifying circuit analysis and design.

From the ideal circuit diagram (Figure 1), the operation of the push–pull converter is determined by three modes of operation, depending on the state of the power switching devices (Mode 1: Q_1 ON and Q_2 OFF, Mode 2: Q_1 OFF and Q_2 ON and Mode 3: Q_1 and Q_2 OFF).

In modes 1 and 2, the conduction of the power switching device allows current to flow through the corresponding primary winding of the transformer (see Figure 1), magnetising its core. This induces a voltage in the secondary circuit of polarity defined by the point criterion (see Figure 1), which will allow current to flow through one of the branches (through diodes D_1 or D_2) to the output low-pass filter and the load R.

Finally, during mode 3 operation, the deactivation of both power switching devices prevents current flow through the primary windings, and hence no voltage will be induced in the transformer secondary circuit (see Figure 1). In this case, it is the output low-pass filter (L_F and C_F) which maintains the output voltage by supplying current to the load. Assuming a continuous conduction mode (CCM) in the output low-pass filter inductor current, it follows that D_1 and D_2 conduct at the same time and there is current sharing between the two branches.

2.2. Non-Ideal Push–Pull Converter Circuit

The electrical circuit in Figure 1 allows modelling the ideal behaviour of the push–pull converter, which is a simple approximation of the actual converter behaviour. To develop an accurate model of the converter, non-idealities associated with the transformer, the power switching devices and the converter output low-pass filter must be considered. With this in mind, the authors developed and validated in [17] the non-ideal model shown in Figure 2, which the authors demonstrated exhibits behaviour very close to the actual circuit of a push–pull converter.

The non-idealities in Figure 2 are as follows (please see list of nomenclature and symbols in this document): for the transformer, the series resistance and the leakage inductances and capacitances of the primary and secondary windings (R_{L_P}, R_{L_S}, $L_{P_{1,2}}$, $L_{S_{1,2}}$, $C_{P_{1,2}}$ and $C_{S_{1,2}}$, respectively) as well as the core losses associated with the magnetisation current, eddy currents and parasitic fluxes (L_M and R_{Nu}) have been considered.

For power transistors (Mosfets), series drain-sink saturation resistance (R_{DS}) and parallel output capacitances ($C_{OSS_{1,2}}$) are considered. For rectifier diodes, the series resistance (R_D) and threshold voltage (V_γ) are considered.

Finally, for the converter output LC filter, series resistance of both the inductance (R_{L_F}) and the filter capacitor (R_{C_F}) are considered.

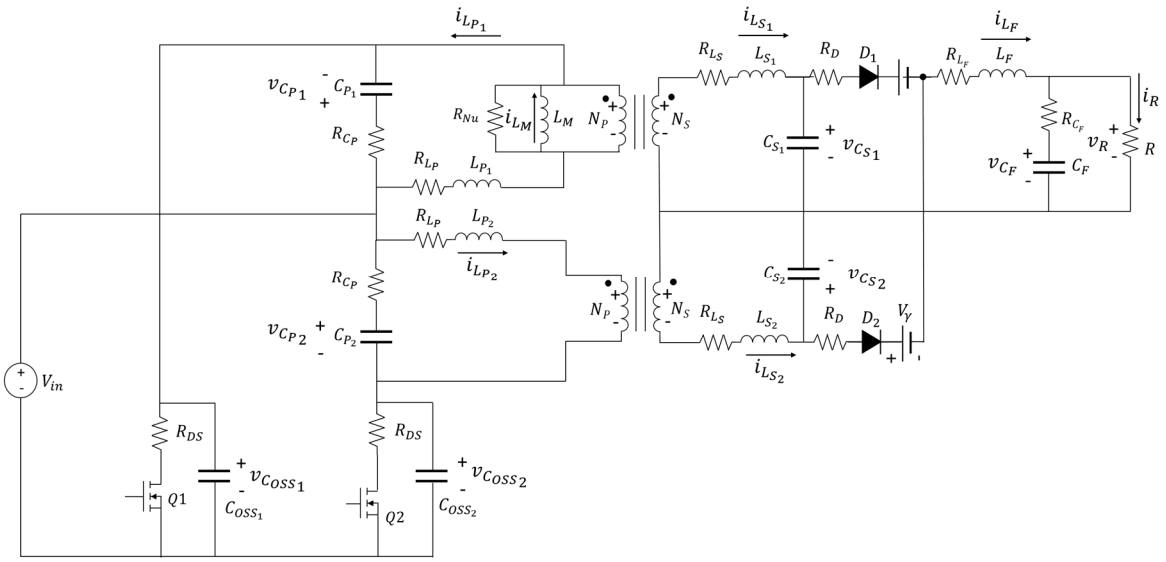

Figure 2. Non-ideal electrical circuit of the push–pull converter of Figure 1.

As stated in [17], because they are considered non-idealities of negligible effect, mainly because they can be avoided with a good design and manufacture of the converter, the following is assumed: As for the transformer, both windings will be identical. In terms of operation, the transformer shall be considered to be fully magnetised and demagnetised in each operating cycle. Likewise, the transformer core will always operate within the linear region of the magnetisation curve, so no core saturation effects will be considered.

Similarly, in the case of power switching devices, it will be considered that the switching times will be negligible with respect to the duty cycle corresponding to the operating frequency. It is also assumed that the power switching devices will be of adequate quality, so their leakage currents will be neglected.

Based on the above, for the complete definition of the non-ideal behaviour of the push–pull converter, the following 14 non-idealities will be considered: $R_{L_P}, R_{L_S}, L_{P_x}, L_{S_x}, C_{P_x}$, C_{S_x}, L_M, R_{Nu}, R_{DS}, C_{OSS_x}, R_D, V_γ, R_{L_F} and R_{C_F}.

2.3. Non-Ideal Push–Pull Model

The non-ideal model of the converter is obtained from the analysis of the non-ideal equivalent circuit shown in Figure 2 for the operating sequences of the power transistors. Thus, following the modelling proposed in [17] and considering as state variables the inductor currents ($i_{L_{P_1}}, i_{L_{P_2}}, i_{L_M}, i_{L_{S_1}}, i_{L_{S_2}}, i_{L_F}$) and the capacitor voltages of the circuit ($v_{C_{P_1}}, v_{C_{P_2}}, v_{C_{OSS_1}}, v_{C_{OSS_2}}, v_{C_{S_1}}, v_{C_{S_2}}, v_{C_F}$), the input voltage of the converter as the input of the model (v_{in}) and the converter output voltage and current as the output variables (v_R, i_R), the complete non-ideal model of the push–pull converter calculated in [17] can be written in its state-space representation according to (1):

$$\begin{aligned} \boldsymbol{x}(k+1) &= \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}u(k) + \boldsymbol{E} \\ \boldsymbol{y}(k) &= \boldsymbol{C}\boldsymbol{x}(k) + \boldsymbol{D}u(k) \end{aligned} \tag{1}$$

where k is the sampling time, the matrices $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, $\boldsymbol{D}$ and $\boldsymbol{E}$ can be found in [17], and

$$\boldsymbol{x} = \left[i_{L_{P_1}}, i_{L_{P_2}}, i_{L_M}, i_{L_{S_1}}, i_{L_{S_2}}, i_{L_F}, v_{C_{P_1}}, v_{C_{P_2}}, v_{C_{OSS_1}}, v_{C_{OSS_2}}, v_{C_{S_1}}, v_{C_{S_2}}, v_{C_F} \right]^T$$

$$u(k) = v_{in}(k)$$

$$\boldsymbol{y}(k) = [v_R(k) i_R(k)]^T$$

3. Push–Pull Converter Sizing and Parameterisation

This section presents the step-by-step methodology to obtain the parameters of the non-ideal model of Figure 2 according to Equation (1). Since the main objective of the paper is to evaluate and identify the impact that each non-linearity has on the overall behaviour of the converter output variables, the methodology developed here is based on a compendium of equations proposed and validated in the scientific literature. In order to avoid continuous cuts in the explanations, the meaning of all parameters and variables used in this section can be found in the list detailing the nomenclature and symbols used in this document.

3.1. Transformer Sizing and Parametrisation

3.1.1. Transformer Core

When sizing a transformer, many variables are involved to estimate the proper core size. It is a complex task that requires consideration of the non-linear relationship of the operating power with respect to the area product, core volume and heat dissipation capacity [29]. To facilitate this task, magnetic core manufacturers propose their own methodology for the correct choice of core size for various applications. These methodologies are based on the determination of the minimum core area product (AP), defined by the area of the magnetic section (A_E) and the window area (A_W) which guarantees the required magnetic flux capacity of the transformer core, assuming its operation in the linear region, for a design power and frequency [30]. In this case, the empirical Equation (2), provided by Unitrode® (Merrimack, NH, USA) and Texas Instruments® (Dallas, TX, USA), will be used to size the cores for the different cases under study. This equation is commonly used in the design of power transformers for switching power supplies [29].

$$AP = A_E \cdot A_W = \left(\frac{P_o}{K \cdot \Delta B \cdot f_{sw}} \right)^{\frac{4}{3}} \tag{2}$$

For the design of the different transformers, E-type core (widely used in the design of power transformers) of N27 and N87 ferrite materials (MnZn) from TDK Electronics® (Munich, Germany) have been chosen. Zinc-based ferrites are characterised by high saturation flux densities and high magnetic permeability, which favours the reduction of core size and cost [31]. The choice of TDK Electronics® products is justified by the fact that it is a well-known manufacturer in the industry, which also has intuitive and powerful design tools for the calculation of the main parameters of the transformer core.

3.1.2. Number of Primary and Secondary Winding Turns

To calculate the number of turns of the primary and secondary windings of the transformer, Faraday's law given by Equation (3) will be used. This equation allows to obtain the value of the induced voltage (V) for an inductor with N turns [9]:

$$V = -N \frac{\Delta \Phi}{\Delta t} \tag{3}$$

Particularly for the study of the primary winding, considering that $\Delta t = t_{on}$ and omitting the minus sign, since it only defines the polarity of the induced voltage, (3) can be written as (4):

$$V_P \cdot t_{on} = N_P \cdot \Delta \Phi = N_P \cdot \Delta B \cdot A_E \tag{4}$$

Then, considering that $t_{on} = \delta / f_{sw}$, (4) can be written as (5):

$$N_P = \frac{V_P \cdot \delta}{\Delta B \cdot A_E \cdot f_{sw}} \tag{5}$$

The number of turns of the secondary winding must guarantee the correct conversion ratio of the transformer considering the operating conditions of the converter. Thus, for its

calculation, both the ratio between input and output voltage and the predefined maximum duty cycle (δ_{max}) shall be considered, according to (6).

$$\frac{N_S}{N_P} = \frac{V_o}{2V_{in}\cdot\delta_{max}} \rightarrow N_S = \frac{N_P\cdot V_o}{2V_{in}\cdot\delta_{max}} \tag{6}$$

3.1.3. Primary and Secondary Windings' Resistance

The resistance value of the primary and secondary windings is determined by their length, effective cross-section and operating temperature according to Equation (7) [32]:

$$R_w = \left(\rho\frac{l_w}{S_w}\right)\left(1+\alpha\cdot\left(T - T_{Ref}\right)\right) \tag{7}$$

The wire length shall be determined by the number of turns of each winding and the core size. Its section will be calculated from the maximum operating current (thermal criterion) that guarantees the integrity of the electrical insulator. In this case, a thermal increase of 60° has been considered for a reference ambient temperature of 20° (maximum operating temperature in permanent regime of 80 °C).

The sizing of the cross-section by thermal criteria depends mainly on the operating current, the arrangement of the conductors in the winding, the number of layers, the thermal resistance of the transformer core, etc. Therefore, it is not easy to obtain a general formulation for the different converter designs. However, since this is not an objective of this work, it has been chosen to use typical experimental effective amperage-section tables for single-pole copper conductors. The values provided by these tables are quite conservative since their determination is based on stringent experimental safety factors.

Finally, to obtain the corrected resistance of the wire, the influence of the frequency on the effective cross-section according to the skin effect will be considered. Knowing the electron decay equation in the conductor cross-section modelled in (8) [33] and assuming that the electrons are concentrated in the effective area given by the skin depth (ξ), a correction factor (κ) of the resistance as a function of the wire cross-section (S_w) and the effective cross-section of the wire (S_{w_e}) can be calculated in (9):

$$\xi = \sqrt{\frac{2\rho}{(2\pi f_{sw})(\mu_0\mu_r)}} \tag{8}$$

$$\kappa = \frac{S_w}{S_{w_e}} = \frac{\pi r^2}{\pi\left(r^2-(r-\xi)^2\right)} = \frac{r^2}{\left(r^2-(r-\xi)^2\right)} \tag{9}$$

In view of the above, the effective resistance values of the winding considering skin effect are given by (10):

$$R_{w_e} = \kappa\cdot R_w \tag{10}$$

3.1.4. Leakage Inductances of Transformer Primary and Secondary Windings

The calculation of the leakage inductance of a transformer (L_{lk}) is a complex task that is highly dependent on the transformer topology, the winding process and the physical separation between conductors. The influence of these factors determines the three fundamental components of the leakage inductance: the internal leakage inductance (L_{in}), the Yoke leakage inductance (L_y) and the equivalent leakage inductance (L_{eq}) [34].

For a transformer with push–pull topology (separate primary and secondary windings), several works have proposed an analytical solution to determine the fundamental components of the leakage inductance of the transformer windings. A general expression for its calculation, successfully validated experimentally, is proposed in [34] and given by (11):

$$L_{lk} = 2\left(L_{in} + L_y + L_{eq}\right) \tag{11}$$

The expressions proposed in [34] for the calculation of internal leakage inductances and yoke leakage inductances are complex and require previous tests on the transformer, so practical simplifications are required, which, with reasonable accuracy, favour their calculation. Thus, if it is assumed that the primary and secondary windings of the transformer are concentric throughout the window area of the central branch of the transformer core (usual in this type of power transformer) and conductors with reduced insulation thickness (insulating varnish) have been used for their manufacture, the terms associated with the internal leakage inductance and the yoke leakage inductance can be considered negligible with respect to the equivalent leakage inductance term [34]. Therefore, the leakage inductance of the transformer windings ($L_{P_{1,2}}$ and $L_{S_{1,2}}$, see Figure 2) can be calculated from the equivalent leakage inductance equation for this type of transformer topology, according to (12) [34]:

$$L_{P,S} = \frac{2 \cdot \mu_0 \cdot N_{P_x,S_x}^2 \cdot l_a \cdot b_w}{3 \cdot h_w} \tag{12}$$

3.1.5. Parasitic Capacitances of Transformer Primary and Secondary Windings

The transformer primary and secondary inductor windings have a distributed parasitic capacitance defined by the turn-to-turn capacitance between turns of the same layer (C_{tt}), between turns of adjacent layers and between turns and the transformer core shield (if present) [35,36]. The total turn-to-turn distributed capacitance of the primary and secondary windings (C_{P_x}, C_{S_x}, respectively; see Figure 2) can be modelled by a parallel capacitance connected between the winding terminals whose value will depend on the thickness of the wire insulation and the winding method used, according to the empirically derived expression (13) [35,36]:

$$C_{tt} = \in_0 \cdot l_t \left(\frac{\in_r \cdot \varnothing}{ln \frac{D_0}{D_c}} + cot\left(\frac{\varnothing}{2}\right) - cot\left(\frac{\pi}{12}\right) \right) \tag{13}$$

where

$$\varnothing = arcos\left(1 - \frac{ln \frac{D_0}{D_c}}{\in_r}\right) \tag{14}$$

To obtain the value of the total parasitic capacitance of the transformer primary and secondary windings (C_{P_x}, C_{S_x}, respectively), it is necessary to consider the number of winding layers. Expression (15) gives an estimate of the total parasitic capacitance of the windings as a function of the number of winding layers [35,36]:

$$C_{P_x}, C_{S_x} = \begin{cases} 1.8300\ C_{tt}\ \text{(for single-layer winding)} \\ 1.3660\ C_{tt}\ \text{(for two-layer winding)} \\ 0.5733\ C_{tt}\ \text{(for three-layer winding)} \end{cases} \tag{15}$$

3.1.6. Magnetising Resistance

For the calculation of magnetising resistance (R_{Nu}, Figure 2), it is necessary to know the core losses. In the scientific literature, there are different analytical models for the estimation of transformer core losses considering Eddy current losses and hysteresis losses, depending on the type of magnetic core and topology [37,38]. These models are complex to apply and require information obtained from experimental tests on the transformer, which makes them difficult to apply in this study. There are simpler and reasonably accurate traditional models that do not require prior testing to estimate power losses. These simplified models are based on generalised experimental equations, such as the experimental Steinmetz equation (OSE), its modified version (MSE), its general version (GSE) or the improved generalised Steinmetz equation (IGSE) [39,40]. For this study, since real transformers are not available for testing and analysis, to obtain the best possible approximation, core losses were estimated from TDK Electronics® transformer and inductance design software

(EPCOS Magnetic Design Tool Ver. 5.5.1.127, compiled on 18 April 2018). The power loss density in the transformer core was calculated considering it to be of the ferrite type, push–pull topology with a duty cycle of 0.45 and a rate operating temperature of 80 °C (usual operating temperature under rate conditions). Considering the power loss density (P_L) at the rated operating voltage of the transformer and considering the voltage drops in the primary windings of the transformer negligible, the magnetising resistance of the transformer core is given by the expression of the active power dissipated in a resistor, given by (16).

$$P_L \cdot V_e = \frac{V_{L_{Nu}}^2}{R_{Nu}} \rightarrow R_{Nu} = \frac{V_{L_{Nu}}^2}{P_L \cdot V_e} \tag{16}$$

3.1.7. Magnetising Inductance

To calculate the magnetisation inductance of the transformer, according to the basic theory of magnetic components, the electrical-magnetic equivalence of the transformer core (reluctance model) is considered [7,41]. For an E-type core without a gap, an equivalent electrical circuit with three reluctances is obtained (Figure 3). Their values are determined according to the dimensions of the transformer core and its magnetic permeability according to Ohm's law (17):

$$\Re_x = \frac{l_x}{A_x \cdot \mu_0 \cdot \mu_r} \tag{17}$$

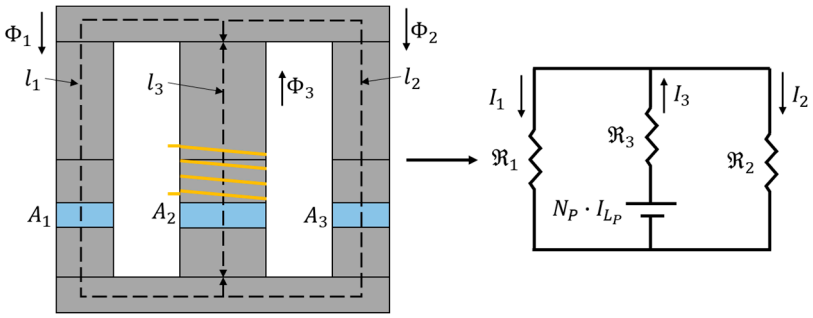

Figure 3. Reluctance model.

Based on the transformer reluctance model (Figure 3) and Ampere's law, expression (18) calculates the total magnetic flux intensity:

$$\Phi_3 = \frac{N_P \cdot I_{L_P}}{\Re_3 + (\Re_1 \parallel \Re_2)} \tag{18}$$

From the concept of inductance, assuming that the transformer leakage inductances are negligible with respect to the value of the magnetising inductance, its value is given by (19):

$$L_M = \frac{\Phi_3 \cdot N_P}{I_P} = \frac{N_P^2}{\Re_3 + \frac{\Re_1 \cdot \Re_2}{\Re_1 + \Re_2}} \tag{19}$$

where

$$\Re_1 = \frac{l_1}{A_1 \cdot \mu_o \cdot \mu_r}, \Re_2 = \frac{l_2}{A_2 \cdot \mu_o \cdot \mu_r}, \Re_3 = \frac{l_3}{A_3 \cdot \mu_o \cdot \mu_r} \tag{20}$$

3.2. Sizing and Parameterisation of the Output Low-Pass LC Filter

3.2.1. Low-Pass Filter Inductance

According to Faraday's law and the operation of the converter, when any of the transistors is on, the relationship between current and voltage at L_F (see Figure 2) is given by (21):

$$v_{L_F} = L_F \frac{di_{L_F}(t)}{dt} = L_F \frac{\Delta I_{L_F}}{\Delta t} \tag{21}$$

If the internal voltage drops associated with the rectifier diodes, power transistors and transformer primary and secondary windings are neglected (considering ideal components is enough for this analysis), the inductor voltage can be obtained by the difference between the voltage induced in the transformer secondary and the converter output voltage. The transformer secondary voltage can be obtained from the product of the converter input voltage and the transformer ratio (22):

$$\frac{\Delta I_{L_F}}{\Delta t} \approx \frac{\left(V_{L_{S_x}} - V_O\right)}{L_F} = \frac{\left(\frac{N_S}{N_P} V_{in} - V_O\right)}{L_F} \tag{22}$$

If $\Delta t = t_{on} = \delta / f_{sw}$, (22) can be written as (23):

$$L_F = \frac{\left(\frac{N_S}{N_P} V_{in} - V_O\right)\delta}{\Delta I_{L_F} \cdot f_{sw}} \tag{23}$$

From (23), the inductance value is inversely proportional to the current ripple in the inductor. For its sizing, the direct relationship between inductance and internal resistance has been considered. In view of the above, to reduce the internal resistance of the inductor, a relatively high-current ripple (ΔI_{L_F} = 30%) has been considered. This ripple value can be easily damped with a high-capacity output capacitor (with much lower internal resistance values).

3.2.2. Low-Pass Filter Capacitance

Considering the charge variation in a capacitor, the relationship between current and voltage at C_F (see Figure 2) is given by (24):

$$i_{C_F} = C_F \frac{di_{V_{C_F}}(t)}{dt} = C_F \frac{\Delta V_{C_F}}{\Delta t} \tag{24}$$

Again, if $\Delta t = t_{on} = \delta / f_{sw}$, if the internal voltage drop of the capacitor is neglected (considering ideal components is sufficient for this analysis) and knowing that the capacitor current is that corresponding to the inductor current ripple, C_F is given by (25):

$$C_F = \frac{I_{C_F} \cdot \delta}{\Delta V_{C_F} \cdot f_{sw}} \tag{25}$$

From (25), the capacitance value is inversely proportional to the voltage ripple in the capacitor. Knowing that it is essential to keep the converter output voltage stable, a voltage ripple value usually used in power supplies (ΔV_{C_F} = 1%) has been considered.

3.3. Sizing and Parameterisation of the Switching Devices

The main criterion used for the sizing of the switching devices is based on determining the rated operating voltage and current values according to the topology and case under study. It will also be necessary to consider an appropriate switching frequency to minimise the switching losses.

Thus, for both the power transistor and the rectifier diode, the rated voltage value will be determined by the maximum blocking voltage during turn-off. For the current, two limit values must be defined, the average and the peak current, which define the thermal and physical operating limits of the switching device, respectively. Generally, sizing switching devices according to the average current criterion also ensures compliance with the peak current criterion since in power switching devices the peak pulsating current is usually much higher than the steady-state current (on the order of two to three times higher) [42].

Thus, based on the push–pull converter operation, the transistor blocking voltage (V_{B_Q}) is determined by twice the input voltage (26). The average current ($I_{Q_{Ave}}$) can be calculated from the quotient of the rated design power and the rated input voltage (27).

Finally, the peak current is determined by the maximum instantaneous input current of the converter, which is highly dependent on the current ripple imposed by the primary leakage and magnetisation inductances of the transformer:

$$V_{B_Q} = 2 \cdot V_{in} \tag{26}$$

$$I_{Q_{Ave}} = \frac{P_O}{V_{in}} \tag{27}$$

In the case of the rectifier diode, the blocking voltage (V_{B_D}) is determined by twice the input voltage multiplied by the transformation ratio (28). On the other hand, the average current ($I_{D_{Ave}}$) can be calculated from the quotient between the rated design power and the output voltage, considering the current sharing between the branches of the full-wave rectifier (29). Finally, the peak current is determined by the maximum instantaneous output current of the converter, which is highly dependent on the current ripple imposed by the low-pass filter inductance:

$$V_{B_D} = 2 \cdot V_{in} \cdot \frac{N_S}{N_P} \tag{28}$$

$$I_{D_{Ave}} = \frac{P_O}{2 \cdot V_{in}} \tag{29}$$

Finally, considering the non-ideal model of the switching devices, the main parameters (see Figure 2), R_{DS} and C_{OSS} for the transistors and V_γ and R_D for the rectifier diodes, can be obtained directly from their datasheets for the expected operating voltage and current conditions.

4. Sensitivity Analysis

4.1. Push–Pull Converter Design: Case Studies

To determine the best trade-off between complexity and practical viability of the model in terms of topology, power and operating frequency, a sensitivity analysis is required to determine the influence of each non-ideality on its dynamic response. Thus, based on Equations (2)–(29), two topologies of push–pull converters, boost and buck, have been designed for four power ranges under study (cases), and three ranges of typical operating frequencies used in the scientific literature and in commercial converters. This determines a total of 24 different converter cases to be studied.

Specifically, for the design of the buck topology, typical voltage values based on single-phase power supplies of 300 VDC input and a converter output of 30 VDC have been considered. In contrast, for the case of the boost topology, practical cases of integration of low-voltage renewable energy sources at 30 VDC input and a converter output of 300 VDC have been considered. Finally, due to the small number of applications, extreme low-power applications (<1 W) and operating frequencies above 500 kHz have not been considered in this study. The four cases under study are as follows:

Case 1: Very low power (1 W–10 W) and operating frequencies of 100 kHz, 300 kHz and 500 kHz.
Case 2: Low power (10 W–100 W) and operating frequencies of 50 kHz, 75 kHz and 150 kHz.
Case 3: Medium power (100 W–1 kW) and operating frequencies of 50 kHz, 75 kHz and 150 kHz.
Case 4: High power (1 W–10 kW) and operating frequencies of 25 kHz, 50 kHz and 75 kHz.

For the sizing of each converter for each topology and case, the design power has been considered as the upper power limit of the case under study, as well as the lowest operating frequency of the established range, being the most restrictive conditions. Likewise, a conservative maximum duty cycle of 0.45 has been considered to avoid short circuits due to operating at duty cycles close to 0.5.

For the design of the different converters according to the established cases and considerations, a market study was carried out based on commercial power electronic devices from widely known manufacturers. From this preliminary study, a first selection of suitable devices was obtained, considering different models but with a similar performance and parameters. Finally, the components were selected considering that their nominal parameters would fit the parameters calculated for each topology, buck and boost, and for each power range under study. Once the components were selected, their main parameters were obtained from the nominal values given in their datasheets in the case of the power switching devices and the output low-pass filter components and from Equations (7)–(20) for the power transformer. Tables 1–4 show the main parameters of the converters designed from the selected components for both topologies and cases.

Table 1. Main parameters of the power converter for case 1.

	Buck Topology		**Boost Topology**	
Element	**Model and Rated Values**	**Parameters**	**Model and Rated Values**	**Parameters**
Output low-pass filter capacitor	MAL211651338E3, VISHAY® (Malvern, PA, USA) 50 VDC	C_F : 3.3 µF R_{C_F} : 3.1 Ω	B32911A3333M000, TDK® (Hutchinson, MN, USA) 50 VDC	C_F : 30 nF R_{C_F} : 1 Ω
Output low-pass filter inductance	SRR1005-151K, Bourns® (Riverside, CA, USA)	L_F : 150 µH R_{L_F} : 520 mΩ	22R156C, Murata Power Solutions® (Westborough, MA, USA)	L_F : 15 mH R_{L_F} : 52 Ω
Transformer	EFD15/8/5, TDK® Ferrite material: N87 Turn ratio: 180:20	N_P : 180 N_S : 20 L_P :13.5 µH L_S :166 nH R_{L_P} : 1.882 Ω R_{L_S} : 53 mΩ C_P :0.67 pF C_S : 1.43 pF L_M : 260 mH R_{Nu} : 320 MΩ	EFD15/8/5, TDK® Ferrite material: N87 Turn ratio: 18:200	N_P : 18 N_S : 200 L_P : 4.2 µH L_S : 52 µH R_{L_P} : 26 mΩ R_{L_S} :2.606 Ω C_P : 1.83 pF C_S :0.36 pF L_M :2.5 mH R_{Nu} : 3.2 MΩ
Output resistance	-	R : 90 Ω	-	R : 9000 Ω
Mosfet	BSS127SSN-7, DiodesZetex® (Plano, TX, USA) 600 VDC, 0.07 A	C_{oss} : 2 pF R_{DS} : 160 Ω	IXTP8N65X2M, IXYS® (Milpitas, CA, USA) 60 VDC, 0.5 A	C_{oss} : 10 pF R_{DS} : 4 Ω
Diode	LL4148, Onsemi® (Scottsdale, AZ, USA) 100 VDC, 0.2 A	V_γ : 1 VDC R_D : 1.875 Ω	US1M-E3/61T, VISHAY® 1000 VDC, 1 A	V_γ : 0.75 VDC R_D : 1.66 Ω

Table 2. Main parameters of the power converter for case 2.

	Buck Topology		**Boost Topology**	
Element	**Model and Rated Values**	**Parameters**	**Model and Rated Values**	**Parameters**
Output low-pass filter capacitor	EEEFN1H680XP, Panasonic® (Osaka, Japan) 50 VDC	C_F : 68 µF R_{C_F} : 680 mΩ	EEEHB1HR68AR, Panasonic® 50 VDC	C_F : 689 nF R_{C_F} : 620 mΩ
Output low-pass filter inductance	PM127SH-330M-RC, Bourns®	L_F : 33 µH R_{L_F} : 57 mΩ	1433507C, Murata Power Solutions®	L_F : 3 mH R_{L_F} : 1428 mΩ
Transformer	E25.4/10/7, TDK® Ferrite material: N87 Turn ratio: 140:16	N_P : 140 N_S : 16 L_P : 85 µH L_S : 1.12 µH R_{L_P} : 300 mΩ R_{L_S} : 7 mΩ C_P : 1.4 pF C_S : 6.9 pF L_M : 330 mH R_{Nu} : 235 MΩ	E25.4/10/7, TDK® Ferrite material: N87 Turn ratio: 14:156	N_P : 14 N_S : 156 L_P : 850 nH L_S : 106 µH R_{L_P} : 24 mΩ R_{L_S} : 663 mΩ C_P : 1.83 pF C_S : 1 pF L_M : 3.3 mH R_{Nu} : 2.36 MΩ

Table 2. *Cont.*

	Buck Topology		Boost Topology	
Element	**Model and Rated Values**	**Parameters**	**Model and Rated Values**	**Parameters**
Output resistance	-	R : 9 Ω	-	R : 900 Ω
Mosfet	STN1HNK60, STMicroelectronics® (Geneva, Switzerland) 600 VDC, 0.4 A	C_{oss} : 20 pF R_{DS} : 8.5 Ω	NDT3055L, Onsemi® 100 VDC, 4 A	C_{oss} : 70 pF, R_{DS} : 100 mΩ
Diode	BYG22D-E3/TR3, VISHAY® 200 VDC, 2 A	V_γ : 1.1 VDC R_D : 300 mΩ	US1M-E3/61T, VISHAY® 1000 VDC, 1 A	V_γ : 0.75 VDC R_D : 1.66 Ω

Table 3. Main parameters of the power converter for case 3.

	Buck Topology		Boost Topology	
Element	**Model and Rated Values**	**Parameters**	**Model and Rated Values**	**Parameters**
Output low-pass filter capacitor	UBT1J221MHD8, Nichicon® (Kyoto, Japan) 35 VDC, 1S3P	C_F : 660 µF R_{C_F} : 53.3 mΩ	EZPE50106LTA, Panasonic® 500 VDC	C_F : 10 µF R_{C_F} : 22 mΩ
Output low-pass filter inductance	IHDM1008BCEV4R7M30, VISHAY®	L_F : 4.7 µH R_{L_F} : 0.95 mΩ	1433445C, Murata Power Solutions®	L_F : 330 µH R_{L_F} : 91 mΩ
Transformer	E42/21/20, TDK® Ferrite material: N87 Turn ratio: 24:3	N_P : 24 N_S : 3 L_P : 3 µH L_S : 46 nH R_{L_P} : 53 mΩ R_{L_S} :1.7 mΩ C_P : 10.6 pF C_S : 11.8 pF L_M : 29.5 mH R_{Nu} :19.8 MΩ	E42/21/20, TDK® Ferrite material: N87 Turn ratio: 3:26	N_P : 3 N_S : 26 L_P : 4 nH, L_S : 309 nH R_{L_P} : 0.6 mΩ R_{L_S} : 92 mΩ C_P : 15.6 pF C_S : 9.5 pF L_M : 462 µH R_{Nu} : 200 kΩ
Output resistance	-	R : 0.9 Ω	-	R : 90 Ω
Mosfet	IXTP8N65X2M, IXYS® 650 VDC, 4 A	R_{DS} : 550 mΩ C_{oss} : 20 pF	RFP50N06, Onsemi® 60 VDC, 50 A	C_{oss} : 600 pF R_{DS} : 22 mΩ
Diode	BYV32E-200,127, WeEn Semiconductors Co., Ltd.® (Shanghai, China) 200 VDC, 20 A	V_γ : 1.15 VDC R_D : 22 mΩ	UF5408-E3/54, VISHAY® 1000 VDC, 3 A	V_γ : 1.25 VDC R_D : 400 mΩ

Table 4. Main parameters of the power converter for case 4.

	Buck Topology		Boost Topology	
Element	**Model and Rated Values**	**Parameters**	**Model and Rated Values**	**Parameters**
Output low-pass filter capacitor	B43464A9688M000, TDK® 400 VDC, 1S2P	C_F : 13.6 mF R_{C_F} : 9 mΩ	C4AQLBW6130A3NK, KEMET® (Fort Lauderdale, FL, USA) 500 VDC	C_F : 130 µF R_{C_F} : 2.4 mΩ
Output low-pass filter inductance	CS-631M-450[a], CoilsWS®	L_F : 630 nH R_{L_F} : 4.5 mΩ	EES55244-131M-45A, CoilsWS® (Orange, CA, USA)	L_F : 130 µH R_{L_F} :6.6 mΩ
Transformer	2xE100/60/28, TDK® Ferrite material: N87 Turn ratio: 1:9	N_P : 9 N_S : 1 L_P : 1 µH L_S : 12.4 nH R_{L_P} : 6.2 mΩ R_{L_S} : 101 µΩ C_P :45 pF C_S : 85 pF L_M : 10.5 mH R_{Nu} : 5 MΩ	2xE100/60/28, TDK® Ferrite material: N87 Turn ratio: 1:9	N_P : 9 N_S : 1 L_P :12 nH L_S : 1.5 µH R_{L_P} : 43 µΩ R_{L_S} : 29 µΩ C_P : 112 pF C_S : 46 pF L_M : 130 µH R_{Nu} : 50 kΩ
Output resistance	-	R : 0.09 Ω	-	R : 9 Ω

Table 4. *Cont.*

	Buck Topology		Boost Topology	
Element	**Model and Rated Values**	**Parameters**	**Model and Rated Values**	**Parameters**
Mosfet	SPW47N60C3FKSA1, INFINEON® (Allentown, PA, USA) 650 VDC, 47 A	C_{oss} : 2200 pF R_{DS} : 70 mΩ	IXFN420N10T, IXYS® 100 VDC, 420 A	C_{oss} : 4390 pF R_{DS} : 2.3 mΩ
Diode	STTH20004TV1, STMicroelectronics® 400 VDC, 240 A	V_γ : 1.325 VDC R_D : 2 mΩ	DSEI30-10A, IXYS® 1000 VDC, 30 A	V_γ : 1.5 VDC R_D : 12.5 mΩ

4.2. Sensitivity Analysis

This analysis consists of a comparison by simulation of the main characteristic parameters associated with the dynamic and steady-state response of the output variable (output voltage, V_O) of a simplified converter model with respect to that of the expected behaviour of the full converter model (reference model) for a step-type input signal.

Due to the nature of the proposed research, it might be considered of interest to work with real converters instead of simulations. However, this would have required the construction of 24 converters. This is an unaffordable cost due to the purchase of devices, acquisition cards, controller circuits, etc. on the one hand and the enormous number of working hours involved on the other. But also, it is not considered necessary, since, as demonstrated in [17], the performance of the complete non-ideal model of the converter fits almost perfectly to the real case. In fact, the complete non-ideal model of the converter was validated against a real converter. Consequently, it is sufficient to use this model, already validated (which can be considered as a reference or benchmark), to analyse the true influence of the non-linearity not taken into account in each case of sensitivity analysis.

The methodology proposed for the sensitivity analysis is based on cancelling out in each simulation of the complete non-ideal model of the converter the effect of a specific non-ideality from those defined in Section 2.2. For this purpose, the terms associated with the non-ideality under study (the one not taken into account in each case) are removed from the full reference model [17], i.e., the corresponding row or column is removed from the model, which reduces the order of (1) from 13 to minus.

In this way, it is possible, by comparison with the full reference model, to isolate the effect that each non-ideality has on the converter response. To quantify this effect, it is necessary to calculate certain magnitudes of percentage errors that determine the differences between the behaviour of the output variable of each simplified model and the reference one (for each non-ideality and case study). Although the reference model is of high order (13th order), the dynamic behaviour of the output parameters, voltage and current is mainly determined by the output low-pass filter (LC circuit). Consequently, the dynamics of the converter output variables can be expected to follow a response similar to that of a second-order system. For this reason, the errors chosen for the analysis are the usual ones in a second-order system: overshoot error, rise time error, fall time error, steady-state error and peak time error. The results of more than 330 simulations performed in a Matlab® Ver R2019a environment for all the cases under study, operating frequencies and topologies, buck and boost are shown in Figures 4 and 5, respectively.

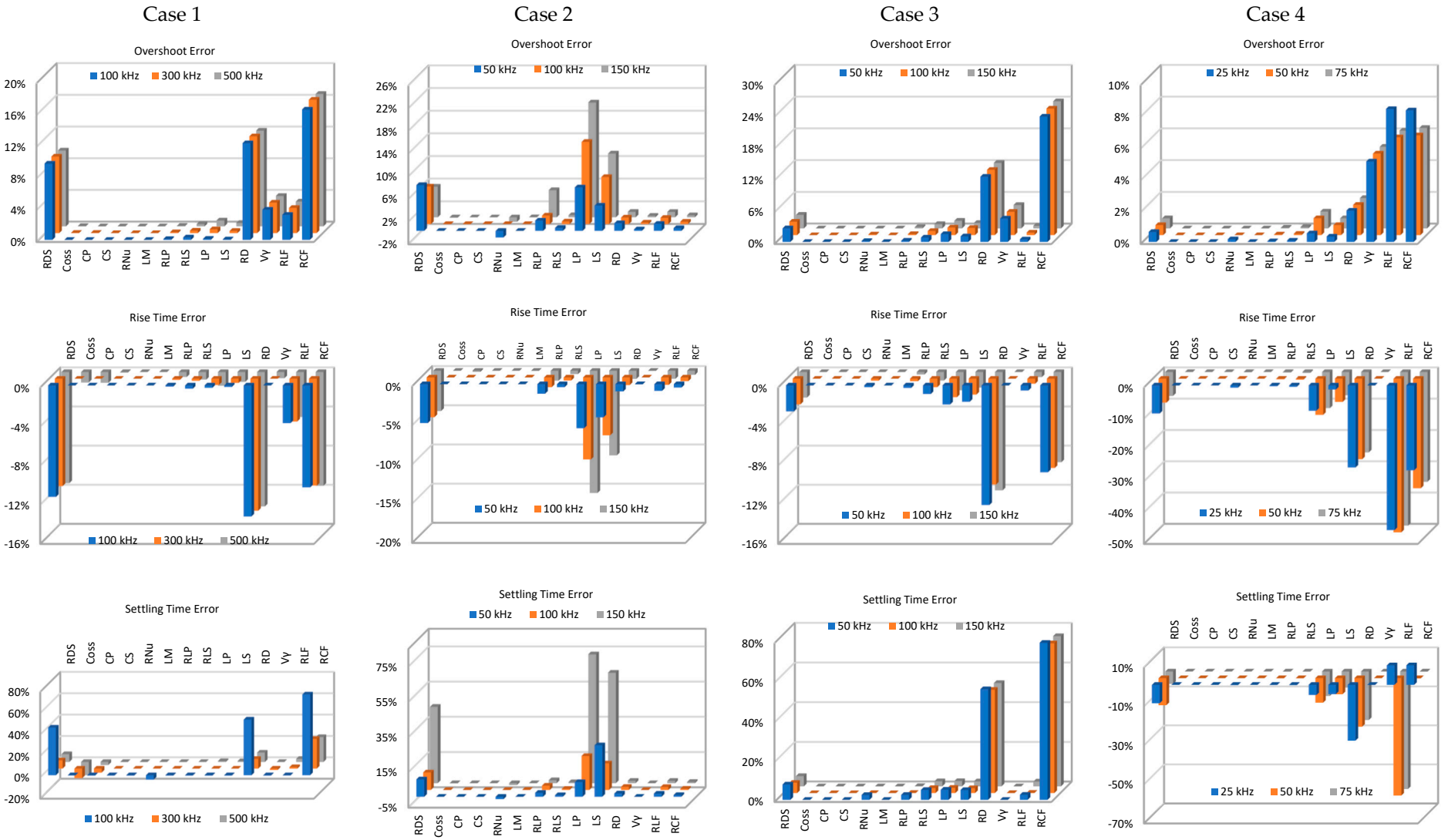

Figure 4. *Cont.*

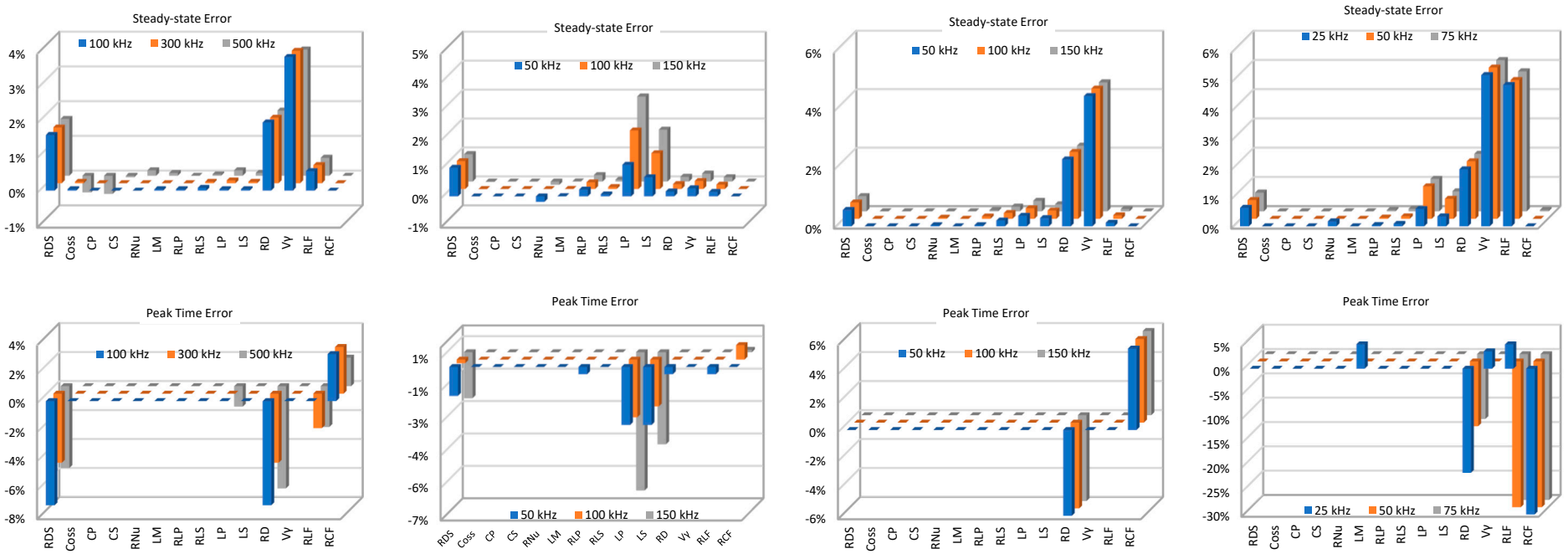

Figure 4. Overshoot error, rise time error, settling time error, steady-state error and peak time error for buck topology in each case.

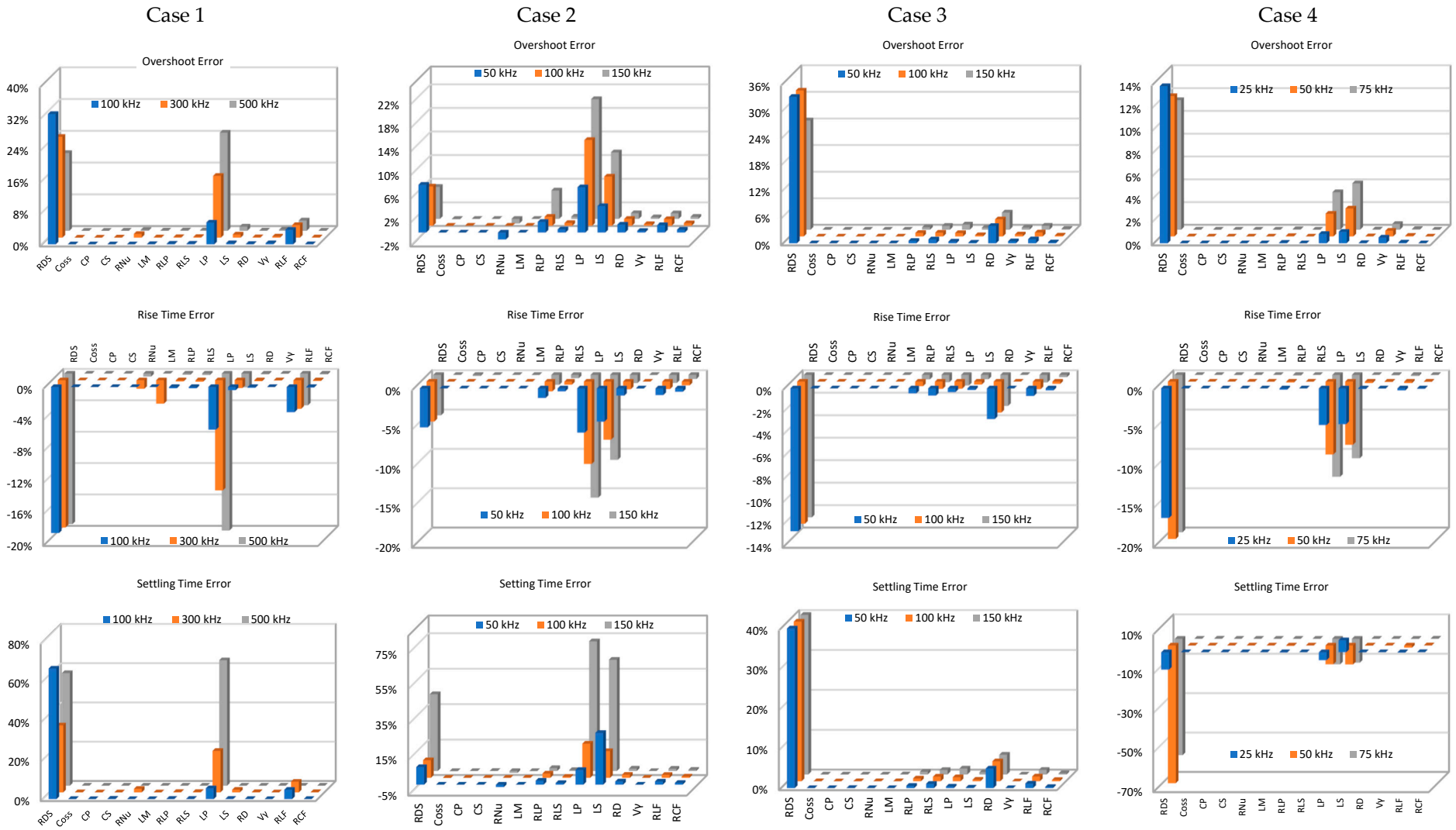

Figure 5. *Cont.*

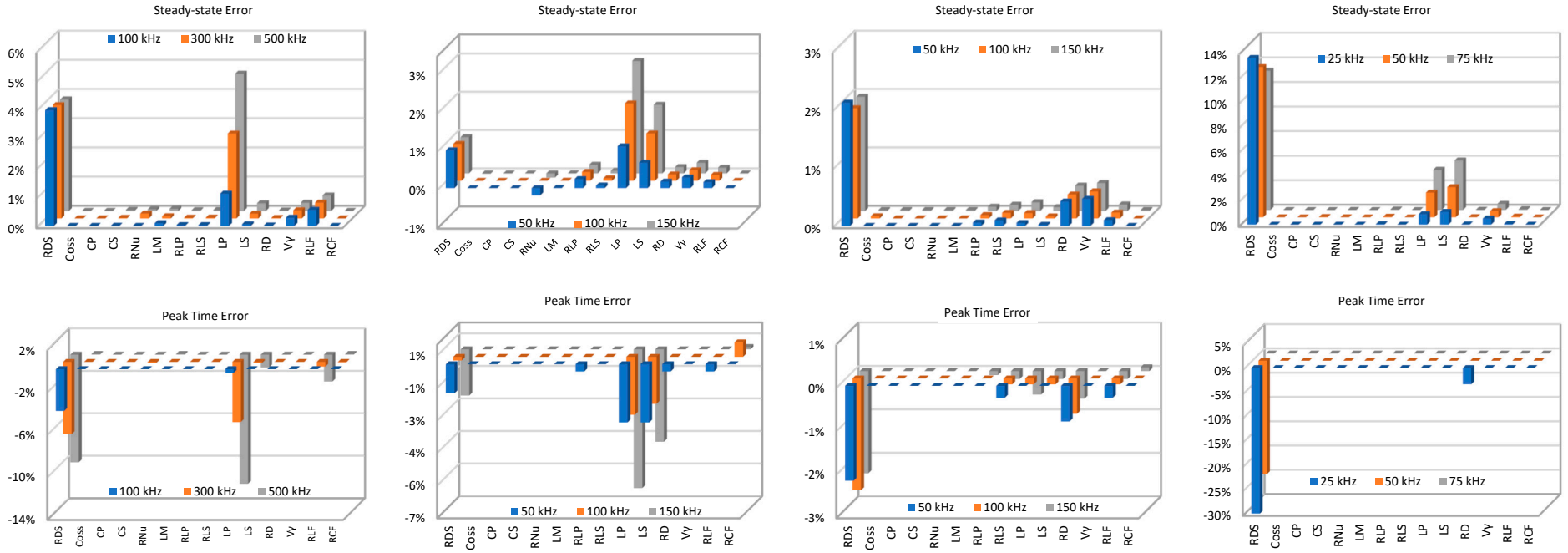

Figure 5. Overshoot error, rise time error, settling time error, steady-state error and peak time error for boost topology in each case.

5. Discussion and Derivation of the Models That Meet the Trade-Off between Complexity and Practical Feasibility

In this section, a detailed analysis of the results obtained from the sensitivity analysis is carried out. In particular, the effects that each non-ideality contributes to the converter behaviour are studied. To this end, an analysis is made of the percentage errors shown in Figures 4 and 5, which quantify the difference in the dynamic and steady-state response of each simplified model (for each non-ideality cancelled) with respect to the expected response (that of the reference model). From this analysis, the key cause–effect relationships are obtained for the subsequent definition of the simplified equivalent circuits of the converter and, ultimately, of the models that fulfil the trade-off between complexity and practical feasibility.

5.1. Discussion

Based on the results obtained from the sensitivity analysis, Figures 4 and 5, conclusions can be drawn to design push–pull converter models that meet the balance between complexity and practical feasibility according to the topology and nominal operating conditions. The effect of each non-ideality on the dynamic and steady-state response of the converter will be analysed element by element. To this end, it is important to note that the dynamic response of the converter's internal variables (voltages and currents), and ultimately the output voltage will be determined by the dynamics provided by the energy storage elements (inductors and capacitors) and the series resistors that limit their charge and discharge dynamics. On the other hand, the steady-state response will be determined both by the voltage drops in resistors and diodes (losses), as well as the influence of the value of the inductances and capacitors. This is justified if it is considered that their values, together with those of the series resistors, determine the variation of the voltage and current variables and, depending on the duty cycle, the final value of these magnitudes.

Firstly, the effect of transformer non-idealities (core and windings) on the response of the converter output voltage will be analysed. Tables 5 and 6 show, easily and qualitatively, the quantitative results of Figures 4 and 5. They show the effect that each non-ideality has on the dynamic and steady-state response of the converter for each topology and case under study. The results of these tables are the basis for the design of the simplified equivalent models of the push–pull converter. Specifically, in Tables 5 and 6, a colour intensity criterion is used to represent the effect that each non-ideality has on the converter output variable: the higher the colour intensity, the greater the effect and vice versa. The criterion for defining the intensity of the effect is as follows: large if any absolute error magnitude is greater than 10%, moderate if it is less than 10% and greater than 5%, reduced if it is less than 5% and greater than 2% and negligible if it is less than 2%.

Considering the transformer core, it is shown that its correct sizing in terms of constituent magnetic material and area product allows the effect of the core non-idealities (L_M and R_{Nu}) on the dynamic and steady-state response of the converter to be negligible (see errors for L_M and R_{Nu} in Figures 4 and 5 and Tables 5 and 6). The reduced influence on the dynamic response is due to the high value of the magnetising inductance (L_M) with respect to those of the windings (L_P). According to expressions (21) and (22), and for the switching frequencies of the converters, its effect on the transformer primary current dynamics and, consequently, on the voltage induced in the secondary is negligible. Finally, the reduced impact on the steady-state response is justified because the losses associated with the core (due to a high value of R_{Nu}) are negligible with respect to the rest of the converter losses.

Similarly, the correct sizing of the transformer primary and secondary winding conductors determines an equivalent resistance (R_{LP} and R_{LS}, respectively) that are negligible with respect to the internal resistances of the power switching devices (R_{DS}). This implies that their influence on the dynamic behaviour of the transformer primary current and, consequently, on the voltage induced in the secondary is very small. Similarly, the reduced values of R_{LP} and R_{LS} imply reduced transformer voltage drops (losses), which determines

the reduced impact on the steady-state response of the output voltage (see errors for R_{LP} and R_{LS} in Figures 4 and 5 and Tables 5 and 6).

Table 5. Influence of model parameters for buck topology in each case.

Buck Topology

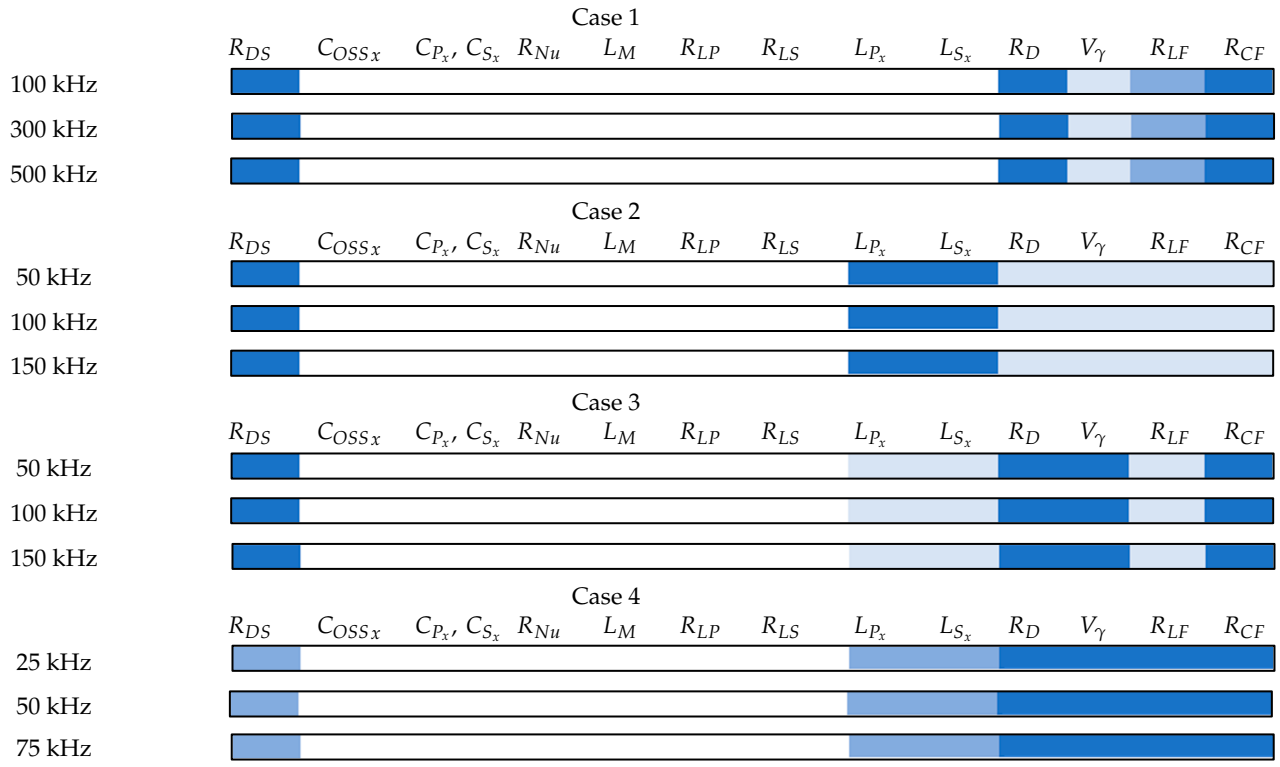

Table 6. Influence of model parameters for boost topology in each case.

Boost Topology

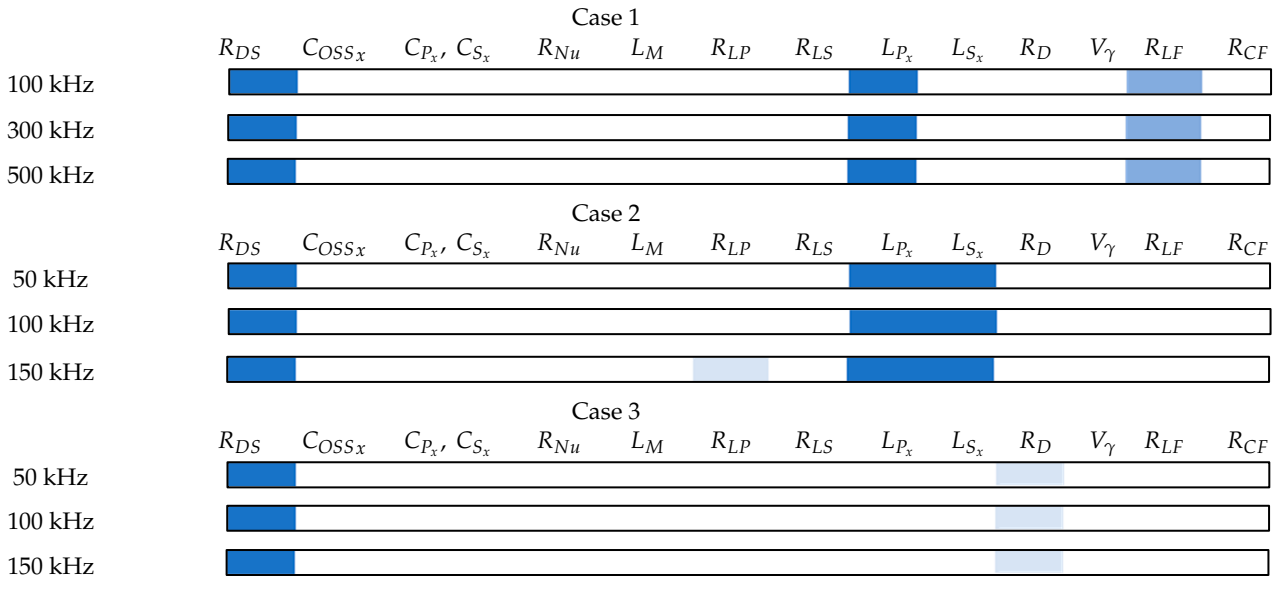

Table 6. *Cont.*

Boost Topology													
Case4													
	R_{DS}	C_{OSS_x}	C_{P_x}, C_{S_x}	R_{Nu}	L_M	R_{LP}	R_{LS}	L_{P_x}	L_{S_x}	R_D	V_γ	R_{LF}	R_{CF}
25 kHz													
50 kHz													
75 kHz													
Legend for colour intensity													
High			Moderate				Reduced				Negligible		

On the other hand, L_P and L_S affect the dynamic and steady-state response of the converter. Considering the effect on both converter topologies, L_P limits the slope of the transformer primary magnetising current due to the opposite induced voltage between its terminals (2): the higher its value, the lower its slope and the induced magnetic flux. This results in a lower induced voltage on the transformer secondary. L_S similarly affects the current dynamics of the transformer secondary circuit. A high value increases the opposite induced voltage at its terminals, which reduces the slope of the secondary current and its final value. This causes variations in the dynamic response and a reduction in the steady-state value of the converter output voltage.

Based on the above, the effect that each non-ideality has on the converter response depends on the value of the self-inductance coefficient of L_P and L_S (highly dependent on the winding method and other factors), the operating frequency and the operating current in both the primary and secondary circuits of the transformer (see errors for L_P and L_S in Figures 4 and 5). Therefore, it is complex to make a statement about the influence of these parameters on a certain topology under certain operating conditions. A general solution is to always consider these non-idealities in the design of the converter model.

Finally, although the values of the leakage capacitances of the transformer windings (C_{P_x} and C_{S_x}) depend on the method of winding the conductors, the number of layers, the insulation thickness, the use of shielding, etc., the values obtained are usually much lower than those of the output capacitances of switching devices and the output filter capacitance (see Tables 1–4). Therefore, their effect on the converter dynamics for the switching frequencies under study can be considered negligible (see errors for C_{P_x} and C_{S_x} in Figures 4 and 5).

Considering the results of the above analysis, the non-idealities of the transformer core (L_M and R_{Nu}),and the winding resistances (R_{LP} and R_{LS}) and leakage capacitances (C_{P_x} and C_{S_x}) can be eliminated from the equivalent simplified model for all cases under study (see Figures 4 and 5). This simplification cannot be applied to the primary and secondary winding leakage inductances (L_P and L_S), whose influence depends on the converter topology, operating power and switching frequency (see Figures 4 and 5).

Considering power switching devices and, first, power transistors (Mosfets), the effect of non-idealities, R_{DS} and C_{OSS_x} will be analysed. As explained above, R_{DS} affects both the dynamic and steady-state behaviour of the converter. The dynamics of the transformer primary variables are determined by the resistors R_{DS} and R_{LP}, which determine the dynamics of the core magnetisation process and the energisation of the transformer primary winding leakage inductances. This follows from the analysis of the RLC circuit generated in the transformer primary by R_{DS}, R_{LP}, L_P and C_{OSS_x} (see Figure 2).

In view of the above, it is the ratio between R_{DS} and R_{LP} which determines their effect on the dynamic behaviour of the converter. An example of this can be seen in the dynamic response for the buck topology cases (Figure 4), where R_{DS}, several orders higher than R_{LP} (see Tables 1–4), imposes the dynamics of the magnetising current flow and has a more noticeable effect on the dynamic behaviour of the converter (see the errors for R_{DS} in Figures 4 and 5 and Tables 5 and 6).

Finally, the effect on the steady-state response is determined by the voltage drop in R_{DS}, which reduces the effective input voltage at the primary of the transformer. This has a negative effect on the voltage induced in the secondary windings and therefore on the steady-state output voltage value of the converter. This effect is more pronounced the higher the operating current of the transistor, i.e., the higher the rated operating power of the converter. These effects can be seen in the results obtained for both topologies, being more prominent for the boost topology, as it operates with higher current in the primary circuit (see errors for R_{DS} in Figures 4 and 5 and Tables 5 and 6).

Although C_{OSS_x} can reach relatively high values compared to the leakage capacitances of the transformer primary windings, it is true that there is a direct relationship between its value and the operating power of the switching device: the higher the working power, the higher the output capacitance (see Tables 1–4). Although this may a priori be a drawback, this is an advantage since for high-power applications their operating frequencies are usually relatively low and makes their effect on the converter dynamics negligible (see errors for C_{OSS_x} in Figures 4 and 5 and Tables 5 and 6).

In the case of the rectifier diode, its internal resistance and threshold voltage influence the steady-state response of the converter, since these non-idealities are reflected as voltage drops (fixed or variable) as a function of the transformer secondary current (see errors for R_D and V_γ in Figures 4 and 5 and Tables 5 and 6). Therefore, its effect is more pronounced in cases where the secondary current is higher. This explains why the effect of R_D and V_γ is greater in the buck topology than in the boost, as well as for the high-power cases, since a voltage drop causes a considerable steady-state error in the output variable, considering the percentage ratio with respect to the nominal output voltage of the converter.

Similar to the effect that R_{DS} has on the dynamics of the transformer primary circuit, R_D together with R_{LS} has an effect on the dynamics of the output low-pass filter energisation process. This is deduced from the analysis of the RLC circuit generated in the transformer secondary by R_D, R_{LS}, L_F and C_F (see Figure 2). In view of the above, it is the ratio between R_D and R_{LS} which determines their effect on the dynamic behaviour of the converter. An example of this can be seen in the dynamic response for the buck topology cases (Figure 4), where R_D, several orders higher than R_{LS} (see Tables 1–4), imposes the dynamics of the output LC filter and has a more noticeable effect on the dynamic behaviour of the converter (see the errors for R_D in Figures 4 and 5 and Tables 5 and 6).

Finally, the effect of the non-idealities associated with the LC output filter will be considered. The non-idealities associated with R_{LF} and R_{CF} have a negative impact on the dynamic and steady-state behaviour of the converter. With respect to the dynamic response, both R_{LF} and R_{CF} influence the dynamics of the energisation process of the low-pass filter inductor and capacitor, respectively. Their effect on the output low-pass filter dynamics depends on the ratio of R_D and R_{LS_x}, as well as the converter operating power and frequency (see Tables 1–4 and the errors for R_{LF} and R_{CF} in Figures 4 and 5 and Tables 5 and 6). The higher their values, the greater the effect on the converter dynamics.

Finally, R_{LF} and R_{CF} affect the steady-state behaviour of the converter due to the voltage drop, which is a function of the current flows in the operation of the low-pass filter. Thus, as with the non-ideality R_D, this effect is proportional to the operating current in the secondary circuit. Therefore, R_{LF} and R_{CF} have a noticeable effect for the buck topology and a negligible one for the boost topology (see errors for R_{LF} and R_{CF} in Figures 4 and 5 and Tables 5 and 6).

5.2. Simplified Models

From the analysis carried out, it is easy to deduce the models that are sufficiently accurate and simpler than the full state-space model developed in [17] (referred to as the reference model). Thus, for the push–pull buck topology, the following non-idealities must be taken into account: switching devices (R_{DS}), HF transformer (L_{P_x} and L_{S_x}), rectifier diodes (R_D and V_γ) and output *LC* filter (R_{LF} and R_{CF}). On the other hand, for the push–pull boost topology, switching devices (R_{DS}), HF transformer (L_{P_x} and L_{S_x}), rectifier diodes

(R_D) and output LC filter (R_{LF}) must be taken into account. Based on the above, the simplified non-ideal equivalent circuits for the push–pull buck and boost topologies are shown in Figure 6a,b, respectively. This allows to simplify the state-space model (1) so that now the state vector will be $x_s = \left[i_{L_{P_1}}, i_{L_{P_2}}, i_{L_{S_1}}, i_{L_{S_2}}, i_{L_F}, v_{C_F}\right]^T$, remaining unchanged with respect to $u(k)$ and $y(k)$. This makes it possible to reduce the model order from thirteen to six. To do this, simply cancel the terms of matrices $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, $\boldsymbol{D}$ and $\boldsymbol{E}$ of the reference (full) model (1) associated with those state variables that are not present in the simplified state vector $\boldsymbol{x_s}$.

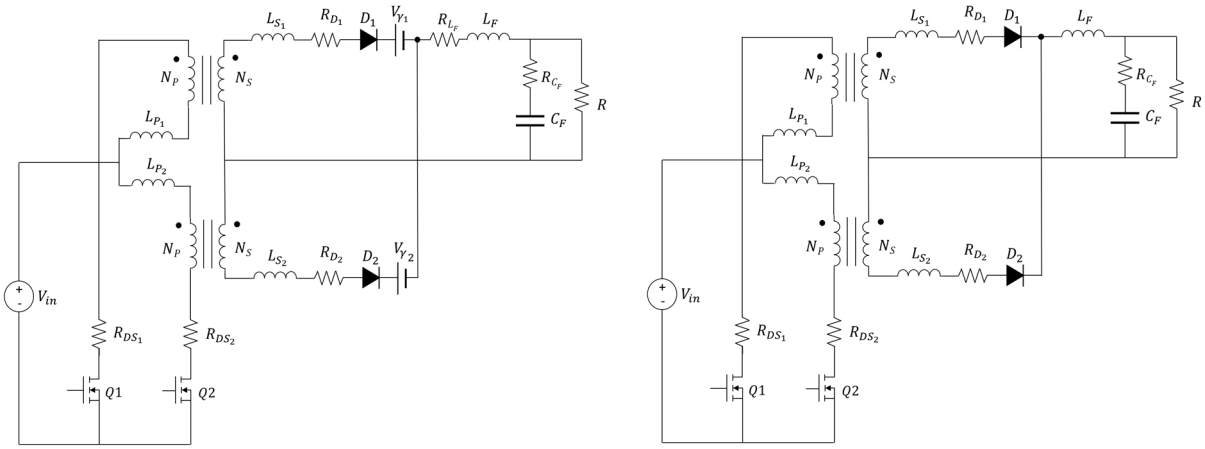

Figure 6. Simplified non-ideal equivalent circuits for (**a**) buck and (**b**) boost topologies, respectively.

Finally, to demonstrate the practical application of the results obtained from the sensitivity analysis, the dynamic and steady-state response of the simplified models was compared with that obtained from the reference model for a step-type input signal.

Figures 7 and 8 show the percentage errors of the dynamic and steady-state response of the simplified models for each case of the buck and boost topologies, respectively. Figure 9 shows the time response and the corresponding validation of the simplified model (Simp) for cases 1 (a) and 4 (b) with respect to the reference model (Ref) and the ideal model (Ideal) for the central values of the switching frequency range for each case and both topologies.

Note that the absolute error percentages shown in Figures 7 and 8 are in all cases lower than five. Likewise, Figure 9 verifies that the dynamic and steady-state behaviour of the simplified models show a similar profile to the reference model and in turn show much higher performances than the ideal model of Figure 1 (the most widespread in the scientific literature).

Based on the results, it is shown that the sensitivity analysis developed for the push–pull converter topology is a very powerful tool for the definition of reduced-order control-oriented models for applications where simplicity and accuracy are fundamental requirements.

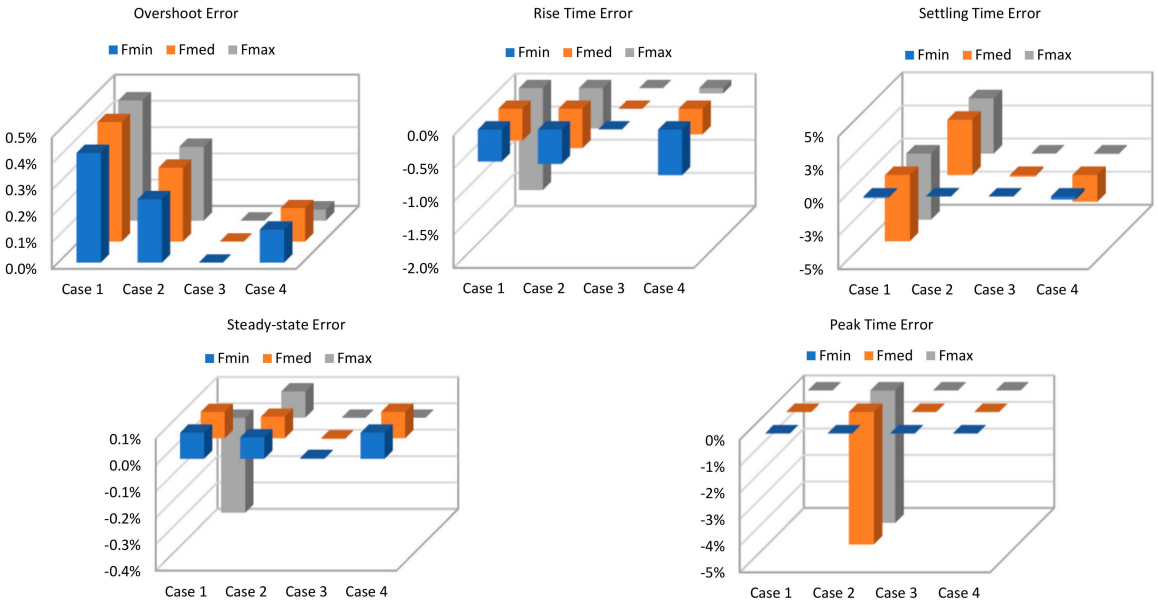

Figure 7. Overshoot error, rise time error, settling time error, steady-state error and peak time error of the simplified models for the buck topology in each case.

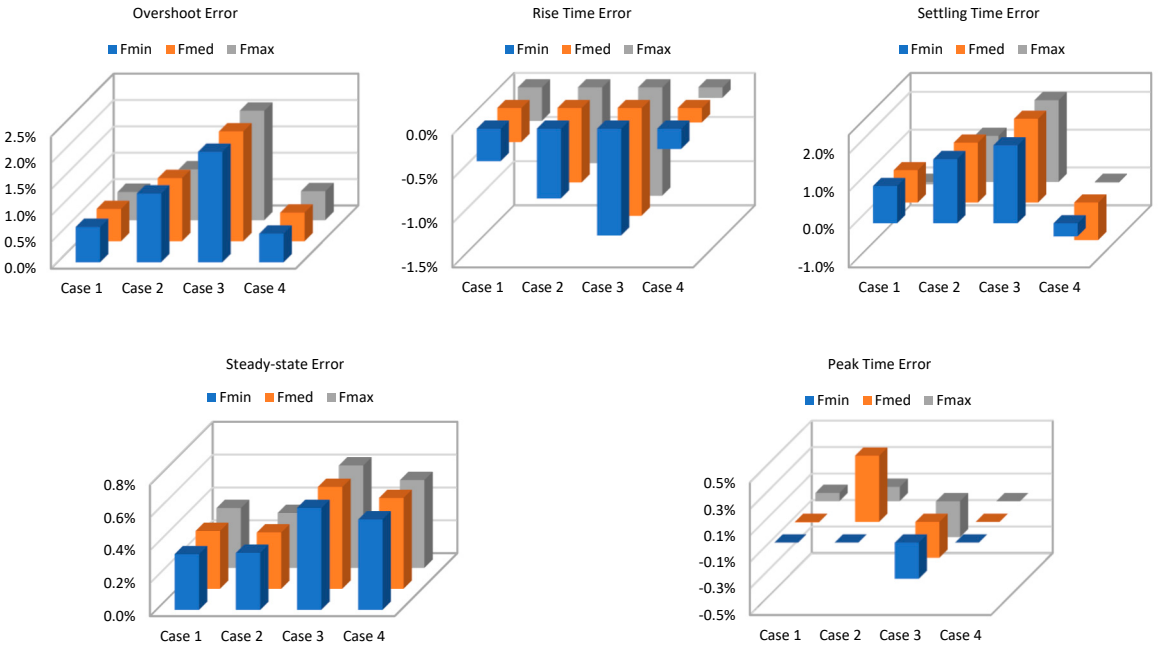

Figure 8. Overshoot error, rise time error, settling time error, steady-state error and peak time error of the simplified models for the boost topology in each case.

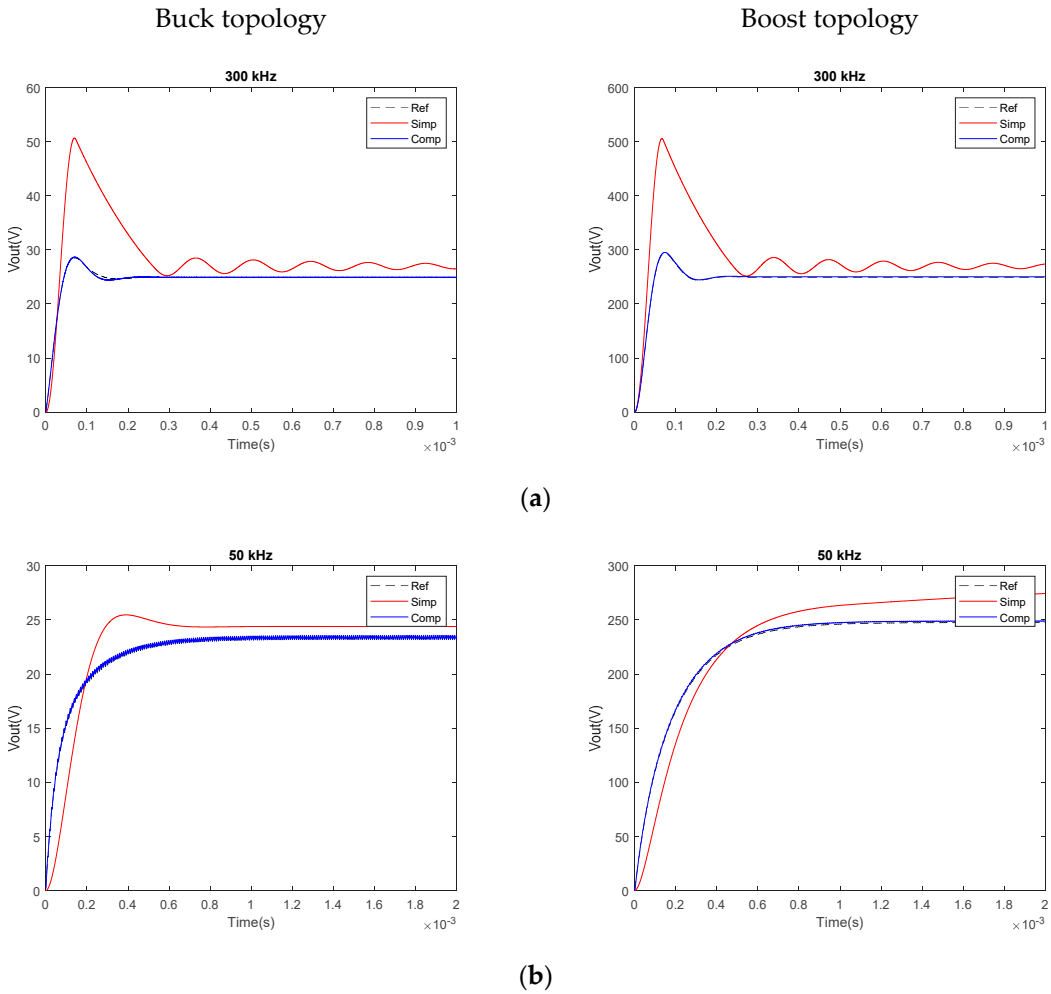

Figure 9. Time response of the simplified model (Simp) with respect to the reference model (Ref) and the ideal model (Ideal) for cases 1 (**a**) and 4 (**b**) for buck and boost topologies, respectively.

6. Conclusions and Future Works

This paper presents a methodology for obtaining simple and sufficiently accurate simplified models of the push–pull converter from its full non-ideal equivalent model.

Unlike the works reviewed in the scientific literature, which present simplified models for specific applications (without general validity), this paper proposes a methodology for obtaining simplified models based on the development of a sensitivity analysis that allows identifying the effect that each non-ideality of the actual (physical) converter has on the response of the simplified model. To obtain these simplified models, the absolute percentage errors of the dynamic response with respect to the reference model behaviour are analysed, considering for their definition those non-idealities whose effect (error) is perceptible in practice.

The performance of the simplified models was evaluated and validated by comparison with respect to the dynamic and steady-state response of the full non-ideal (reference) model, showing absolute percentage errors in all cases below 5%, as well as a dynamic response very similar to that of the reference model.

In view of the analysis carried out, it is concluded that the use of the proposed methodology, based on the use of a sensitivity analysis, allows defining, quantifying and assessing the effect of each non-ideality of the actual (physical) converter to obtain simple and very accurate simplified models of the push–pull converter.

Future work from this research focuses on the application of the simplified models obtained for the design of model-based controllers with the aim of improving the performance of the controller–converter set.

Author Contributions: Methodology, F.J.V.; Software, F.S.; Formal analysis, J.M.A.; Investigation, F.J.V., J.M.A. and F.S.; Writing—original draft, F.J.V. and F.S.; Writing—review & editing, J.M.A.; Supervision, J.M.A. All authors have read and agreed to the published version of the manuscript.

Funding: This work is a contribution of the PID2020-116616RB-C31 Project supported by the Spanish Ministry of Economy and Competitiveness, by the P20_00730 Project supported by Regional Andalusian Government under the European Union Regional Development Fund. Funding for open access charge: Universidad de Huelva/CBUA.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature and Symbols

A_E	Core magnetic cross-section area (cm^2)
α	Temperature coefficient of conductive material ($3.9 \cdot 10^{-3}\ C^{-1}$ for copper)
AP	Core area product (cm^4)
A_W	Window area available for the winding (cm^2)
A_x	Area of E-type transformer reluctance (m^2)
b_w	Core window width along x axis (m)
C_F	Filter capacitor (F)
C_{OSS_x}	Mosfet output capacitance (F); x = 1, 2
C_{P_x}	Parasitic primary winding capacitance (F); x = 1, 2
C_{S_x}	Parasitic secondary winding capacitance (F); x = 1, 2
C_{tt}	Total parasitic turn-to-turn capacitance of the transformer winding (F)
δ	Duty cycle
D_C	Total conductor diameter excluding insulation thickness (mm)
D_x	Output branch circulation diodes; x = 1, 2
D_0	Overall conductor diameter including insulation thickness (mm)
ΔB	Flux density deviation swing (Tesla, T)
ΔI_{L_F}	Filter inductor ripple current (A)
ΔV_{C_F}	Filter capacitor ripple voltage (V)
$\in_0$	Vacuum electric permittivity ($8.8542 \cdot 10^{-15}$ F/mm)
$\in_r$	Relative electrical permittivity of the electrical insulator (3.5)
f_{sw}	Switching frequency (Hz)
h_w	Core window height (m)
κ	Correction factor for the effective conductor cross-section of the windings
$I_{x_{Ave}}$	Average operating current of switching devices (A), x = Q (transistor), D (rectifier diode)
I_{CF}	Filter capacitor current (A)
I_{LF}	Filter inductance current (A)
K	Parameter associated with the converter topology (0.017 in this case)
l_a	Average turn length of secondary windings (m)
L_{eq}	Equivalent leakage inductance (F)
L_F	Filter inductance (H)
L_{in}	Internal leakage inductance (F)
L_{lk}	Leakage inductance of a transformer winding (F)
L_M	Leakage inductance due to core magnetising losses (H)
L_{P_x}	Leakage inductance of the primary winding (H); x = 1, 2
L_{S_x}	Leakage inductance of the secondary winding (H); x = 1, 2
l_t	Turn length (mm)
l_x	Length of E-type transformer reluctance (m^2)

l_w	Length of the windings (m)
L_y	Yoke leakage inductance (F)
μ_0	Vacuum magnetic permeability ($4 \cdot \pi \cdot 10^{-7}$ H/m)
μ_r	Relative magnetic permeability of the conductive material
MPPT	Maximum Power Point Tracking
N_P	Number of turns of the primary winding
N_S	Number of turns of the secondary winding
P_L	Transformer core power losses density (W/m^3)
P_O	Output power of the converter (W)
PV	Photovoltaic
Q_x	Mosfet; x = 1, 2
r	Wire radius of transformer windings (m)
R	Load resistor (Ω)
R_{C_F}	Filter capacitor series resistor (Ω)
R_D	Diode series resistor (Ω)
R_{DS}	Mosfet drain-sink resistance (Ω)
$\Re_x$	Equivalent reluctance of transformer sections (A·t/Weber)
R_{L_F}	Filter inductor series resistor (Ω)
R_{L_P}	Primary winding resistor (Ω)
R_{L_S}	Secondary winding resistor (Ω)
R_{Nu}	Magnetisation resistance related to core losses (Ω)
R_w	Resistance of the conductors of the transformer windings (Ω)
R_{w_e}	Effective resistance of the conductors of the transformer windings (Ω)
ρ	Resistivity of the conductive material ($1.71 \cdot 10^{-8}$ Ω·m for copper)
S_w	Cross-section of the conductive material of transformer windings (m^2)
S_{w_e}	Effective cross-section of the conductive material of transformer windings (m^2)
T	Operating temperature of conductive material (°C)
t_{on}	Activation time of any of the converter electronic switches
T_{Ref}	Reference temperature of conductive material (°C)
Φ	Magnetic flux intensity (Wb)
V_{B_Q}	Blocking voltage of switching devices (V), x = Q (transistor), D (rectifier diode)
V_{C_F}	Filter capacitor voltage (V)
V_e	Transformer core effective volume (m^3)
V_γ	Diode forward voltage (V)
V_{in}	Converter input voltage (V)
V_{LF}	Filter inductance voltage (V)
V_{LP}	Leakage inductance of the primary winding voltage (V)
V_{LS}	Leakage inductance of the secondary winding voltage (V)
V_{RNu}	Magnetisation resistance voltage (V)
V_O	Converter output voltage (V)
V_P	Primary winding voltage (V)
ξ	Skin depth inside the conductor above which the electron flow rate is reduced to 63% (m)

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