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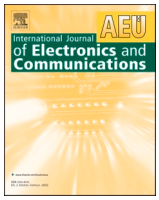

Regular paper

# Simple power-efficient preamplifier-shaper channel for readout interface of silicon detectors

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ABSTRACT

This paper presents the design and characteristics of a front-end readout system for silicon sensors used in nuclear spectroscopy studies. Furthermore, the study proposes circuit topologies that combine gain-boosting and class-AB techniques featuring a good performance regarding gain, accuracy, speed, linearity, and power consumption, meeting the stringent requirements of deep submicrometer CMOS technologies. The readout channel comprises a charge-sensitive amplifier with a tunable discharge time, pole-zero cancellation circuit, and first-order unipolar shaper with a peaking time of 90 ns. The building blocks are made up of single-stage op-amps, thus not requiring compensation. Furthermore, the circuit is optimized for a detector capacitance of 5 pF, and the noise performance is discussed. Experimental results in a 180 nm CMOS process and a supply voltage of ±0.9 V validate the designed front-end channel. The total area of the chip obtained was 0.028 $mm^2$. The conversion gain was 3.1 mV/fC, and the system maintained linearity up to an input charge range of 150 fC with a maximum output swing of 460 mV and recovered to the baseline within 400 ns. The compact design and the power consumption of only 1.97 mW provided a feasible solution for current radiation detectors coupled to many highly dense electronic channels.

## 1. Introduction

Modern radiation detectors are complex mixed-signal systems built from several circuits that perform specific functions, in which the crucial performance is set by the analog circuitry that receives the signal from the sensor [1]. The impinging radiation energy is converted into electricity by a sensor, with the electric signal being initially processed by analog front-end electronics and subsequently by digital circuitry. These types of detectors produce electrical charges and are essential devices in many research areas, such as particle physics, nuclear, astrophysics, space, and medical imaging, thus providing wide application prospects [2–8].

Modern technologies that allow for the development of high-performance systems, high segmentation and large-scale use of modern detector arrays, and experimental complexities demand more compact, high-channel-density systems coupled directly to the detector and low-power electronics wherever possible. Owing to the many channels and wide range of potential requirements, front-end electronics, which receive and process signals directly from sensors, are often fabricated as custom integrated circuits using modern very-large-scale integration (VLSI) technologies. Consequently, in the last decade, microelectronic design in CMOS technologies has marked a trend in the development of readout front-end electronics (FEE), with widespread implementation in hybrid multichannel architectures where analog and digital circuits share the same chip [9–11]. FEE are the electronics located near the detector that manage the analog conditioning of the signals in terms of charge-to-voltage conversion, amplification, pulse-shaping, and analog-to-digital conversion.

The specific requirements of CMOS technology used for analog front-end signal processing distinguish it from those used for digital signal processing [12]. The analog part requires robust technology with low electronic noise and a high dynamic range, typically requiring high power supply voltages. In addition, the existence of many independent channels requires a sensitive area to be segmented to allow highly

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parallelized processing of the resulting signals. This, in turn, demands design simplicity, high speeds, and limited power consumption. Class AB amplifiers maintain low static power dissipation with large output current levels and should be included in building blocks [13–15].

This study focuses on front-end electronics for sensors that detect individual charged particles and approaches circuit solutions to implement the most critical analog building blocks of such systems. The remainder of this paper is organized as follows: Section 2 presents an overview of a conventional readout front-end system. Section 3 presents the proposed topologies of the preamplifier and shaping circuit using gain-boosting and class AB techniques. Section 4 discusses the simulations and experimental results. Finally, the conclusions are presented in Section 5.

## 2. Readout front-end analog processing channel overview

The operation of radiation detectors is based on converting the energy lost by incident particles into electrical signals, which are then processed by appropriate electronics. The first element of a readout system is often an integrated circuit designed to serve a specific purpose (application-specific integrated circuit, ASIC). The design of the ASIC reflects the requirements for processing signals in parallel in an identical manner, that is, to perform amplification, filtering, analog-to-digital conversion, and high-speed data transmission, which enables the integration of complex analog and digital circuits on the same silicon substrate [16]. The general architecture of a front-end system is shown in Fig. 1(a). At the input of each channel, there is an amplifier followed by a filter designed to maximise the signal-to-noise ratio. The signal can be further processed before being digitised and stored in memory until reading. The complexity of some system blocks is application-specific; thus, they can sometimes take simple forms or be omitted entirely. Aspects such as the physics of the process under study, the characteristics of the sensor, or additional constraints such as the power consumption, required number of channels, or space available to fit the system into the condition of the choice of the parameters of the front-end electronics.

Front-end electronics (FEE) are typically produced by cascading several stages. A preamplifier-shaped structure is commonly adopted in the design of the above systems, in which several key parameters are defined by the input amplifier and filter [17]. The conventional block diagram of the detection system is shown in Fig. 1(b).

Regarding signal formation in the detector, a charged particle crossing the sensor interacts with its atoms, creating hole-electron pairs in the semiconductor. The detector is an inversely biased pn junction built with two electrodes. It is connected to a high-voltage supply, which is filtered to reduce noise and is tied to the input of a preamplifier, which is obtained by connecting a suitable network in the feedback path of a high-gain voltage amplifier. This justifies the representation of the detector as a current source $I_d$ with a capacitor in parallel, indicated as $C_d$. The electronic charges from the sensor must be transformed, sorted, analysed, and stored. The total charge contained in the signal is linked to the energy released in the sensor by the impinging quantum radiation. Thus, the basic information of interest is associated with signal amplitude.

The first stage, which is connected directly to the sensor, is the preamplifier, whose core is a voltage amplifier that works as an integrator. In nuclear and particle physics, the obtained detector signals are typically significantly fast pulse signals that are transformed into voltage signals using a preamplifier, whose role is to amplify and preserve the shape of the signal with high fidelity. This requires circuits with significantly large gain and bandwidth and, thus, high power consumption. However, the integration of CMOS technologies implies that each channel must be compact, have a low power budget and low noise, be linear, and adapt to the experiment. A feedback capacitor transforms the charges or equivalent electrical current into voltage. A feedback

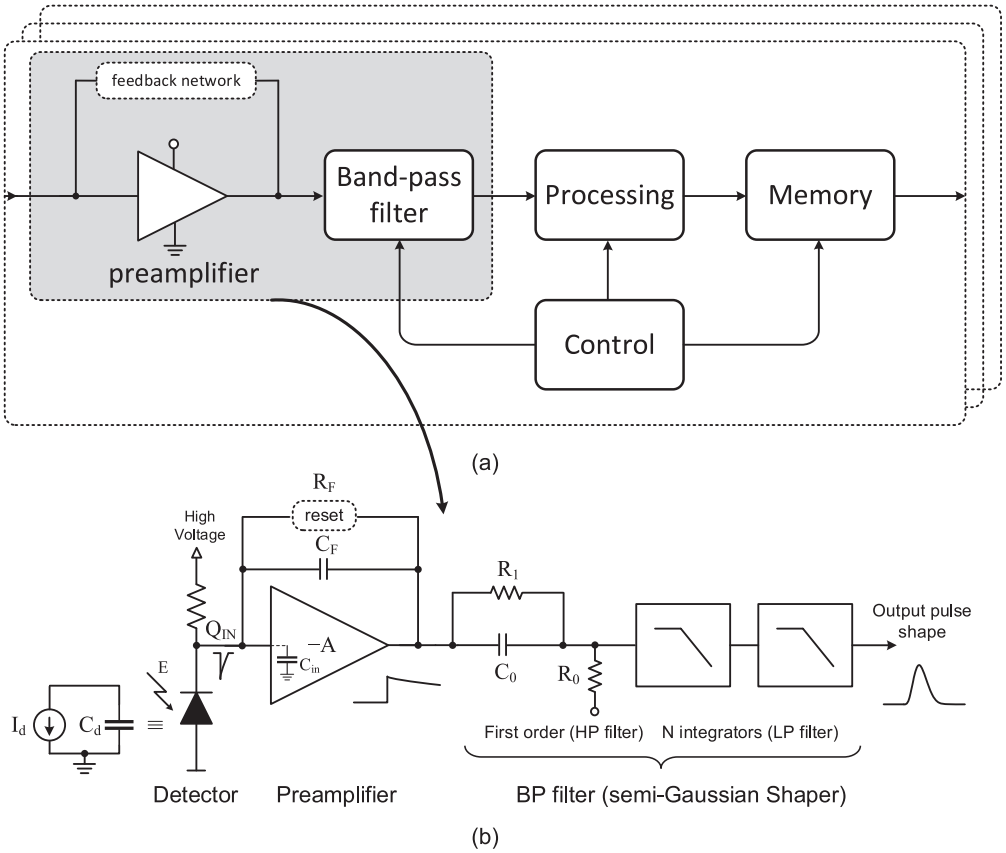



**Fig. 1.** (a) General block diagram for a front-end ASIC. (b) Conventional preamplifier-shaping filter readout front-end system.

switch cuts off the signal and must be used to prevent accidental pile up when new charges arrive. Thus, the generated charge $Q_{IN}$ in the detector is integrated into a small feedback capacitance, which gives rise to a step-voltage signal at the output of the preamplifier with an amplitude equal to $Q_{IN}/C_F$. The architecture used for the preamplifier is also known as a charge-sensitive amplifier (CSA). It is preferred owing to the insensitivity of the gain to the detector capacitance if the open-loop gain $A$ of the core of the preamplifier is sufficiently high:

$$H(s) = -\frac{1}{s}\frac{A}{(A+1)C_F + C_{in}} \approx -\frac{1}{sC_F} \quad if\ A >> 1 \tag{1}$$

where $C_{in}$ includes all the capacitances appearing at the input of the preamplifier, i.e., detector, stray capacitances owing to the connection, and the own operational amplifier. Thus, because the feedback capacitor $C_F$ is a well-controlled component, the previous relationship agrees that the input charge is accurately converted into a voltage pulse. This conversion gain of the CSA is also called the charge gain and is expressed as $(v_{out} / Q_{IN}) = 1/C_F$ (V/pico coulomb). In practice, $C_F$ is selected based on the required conversion gain. Nevertheless, sensitivity is another parameter that is used to express the output of the energy deposited in the detector in mV/MeV. The amount of charge generated is given by $Q_d = E\bullet(e^- / \varepsilon)$, where $E$ denotes the deposited energy (MeV), $e^-$ denotes the electron charge ($1.6 \times 10^{-19}$C), and $\varepsilon$ denotes the energy required to produce a pair of charge carriers in the detector in electron volt. If it is assumed that all of this charge is delivered to the preamplifier, and by using the previous expression for $Q_d$, the output voltage is given by $v_{out} = (E\bullet 1.6\bullet 10^{-19}\bullet 10^{6}) / (\varepsilon\bullet C_F)$, where $\varepsilon = 3.62$ eV for a silicon detector at 300 K and $10^6$ converts the MeV to eV. Therefore, the sensitivity is denoted as $v_{out} /E$ assuming that all charges produced in the detector contribute to the output pulse.

However, the core amplifier has frequency-dependent voltage gain, which in the simplest form with one pole can be written as:

$$\frac{v_{out}(s)}{v_{in}(s)} = A_V = -\frac{A}{1 + s/\omega_0} \tag{2}$$

where $\omega_0$ is the dominant pole of the amplifier. The gain-bandwidth product of the amplifier is $GBW = A\ \omega_0$.

Considering the currents in the input node,

$$i_D(s) = v_{in}(s)\cdot sC_{in} + (v_{in}(s) - v_{out}(s))\left(\frac{1}{R_F} + sC_F\right) \tag{3}$$

yields,

$$\frac{v_{out}(s)}{i_D(s)} \approx -\frac{A}{\frac{1+A}{R_F} + s\left[R_F C_F + \frac{1}{GBW}\right] + s^2\frac{(C_{in}+C_F)R_F}{GBW}} \tag{4}$$

Since $A \gg 1$ and assuming that the requirement $(A + 1)C_F \gg C_d$ is fulfilled, (4) can be rewritten as,

$$\frac{v_{out}(s)}{i_D(s)} \approx \frac{R_F}{1 + s\left[R_F C_F + \frac{1}{GBW}\right] + s^2\frac{(C_{in}+C_F)R_F}{GBW}} \tag{5}$$

The above transfer function has two poles $\omega_1$ and $\omega_2$, which are usually real and widely separated ($\omega_1 \ll \omega_2$). As the denominator of this function can be written as $D(s) \approx 1 + (s/\omega_1) + (s^2/\omega_1\omega_2)$, the dominant pole of CSA is $\omega_1 = 1/(R_F C_F + GBW^{-1}) \approx 1/(R_F C_F)$ because the feedback time constant $R_F\bullet C_F$ is much higher than $1/GBW$. The second high-frequency pole is given by $\omega_2 \approx (GBW\bullet C_F)/(C_{in} + C_F)$. There are two time constants related to the above poles feedback time constant $\tau_f = 1/\omega_1$ and $\tau_2 = 1/\omega_2$, and the transfer function of the CSA can be rewritten as,

$$\frac{v_{out}(s)}{i_D(s)} \approx -\frac{R_F}{(1 + s\tau_F)\cdot(1 + s\tau_2)} = -\frac{1}{C_F}\frac{\tau_F}{\tau_F - \tau_2}\left(\frac{\tau_F}{1 + s\tau_F} - \frac{\tau_2}{1 + s\tau_2}\right) \tag{6}$$

For an input current pulse $i_D(t) = Q_{in}\bullet\delta(t)$ from the detector, the CSA output is [12,18]:

$$v_{out}(t) \approx -\frac{Q_{in}}{C_F}\frac{\tau_F}{\tau_F - \tau_2}\left[e^{\frac{-t}{\tau_F}} - e^{\frac{-t}{\tau_2}}\right] \tag{7}$$

The time constant $\tau_F$ is responsible for the slow signal decay and $\tau_2$ determines the rise time at the CSA output. For very high feedback resistance $R_F \to \infty$, the time constant $\tau_F \to \infty$, and (7) becomes $v_{out}(t) \approx -(Q_{in}/C_F)(1 - e^{-t/\tau 2})$. For a very fast core amplifier $GBW \to \infty$, the time constant $\tau_2 \to 0$ and finite $\tau_F$, the equation simplifies to $v_{out}(t) \approx -(Q_{in}/C_F)(e^{-t/\tau F})$.

Another parameter of the CSA to take into account is the input impedance. For low frequencies it is given by:

$$Z_{in}(s) \approx -\frac{1}{A}\left(\frac{R_F}{1 + sC_F R_F}\right) \tag{8}$$

For high values of $R_F$, the input impedance is capacitive, given by: $C_{in} \approx A\bullet C_F$. However, for high values of $R_F$ and high frequencies, is given by:

$$Z_{in}(s) \approx \frac{s}{GBW}\frac{1}{s\,C_F} = \frac{1}{C_F\,GBW} \tag{9}$$

Thus, the time constant at the input of CSA, $\tau_{in} = R_{in}\bullet C_{in}$ is $\tau_{in} = C_{in} /(C_F \bullet \text{GBW})$. Therefore, the amplifier's bandwidth must be large enough to quickly transfer the charge generated by the detector to the CSA amplifier.

The subsequent stages of the FEE are band-limited and determine the frequency spectrum of the output pulse and its shape, thereby forming a pulse shaper. The time response of the system is tailored to optimise the measurement of either the signal magnitude or the time and rate of signal detection. The output of the signal chain is a pulse whose area is proportional to the original signal charge, that is, the energy deposited in the detector. The pulse shaper transforms a narrow detector current pulse into a broader pulse (to reduce electronic noise) with a gradually rounded maximum at the peaking time (the time taken by the shaper to reach the peak value) to facilitate the amplitude measurement by an analog-to-digital converter. The signal is digital and can be stored and processed.

Literature proves an optimum signal-to-noise ratio can be obtained using a Gaussian-shaped step response. Filters with complex poles designed following the synthesis method reported in [19] achieve a nearly true Gaussian pulse shape. Filter topologies such as multiple feedback topology, Sallen-Key or Bridged-T feedback can be used [18,20]. Nevertheless, the most commonly used pulse shapers in readout systems are semi-Gaussian pulse-shaping filters. A well-known technique uses the CR-RC$^n$ filter to approximate delayed Gaussian waveforms. This type of shaper uses a differentiator followed by $n$ cascaded integrators. The pulse duration is set by a high-pass (HP) filter and a low-pass (LP) filter located posteriorly, increasing the pulse rise time to limit the noise bandwidth. However, a physical system cannot be implemented by using an ideal Gaussian shaper since an infinitely large number of RC integrators is necessary. Increasing the order of the filter makes the pulse more symmetrical and return to the baseline faster, reducing the probability of pulses pile-up in high-rate experiments. A higher filter order requires more power and occupies more silicon area. For that reason, multichannel readout ASICs also use simple CR-RC shapers to save power consumption and die size [21].

## 3. Readout circuit design

Fig. 2 shows the readout channel designed in this work, which is formed by the preamplifier-shaper structure commonly adopted in the design of the above systems.

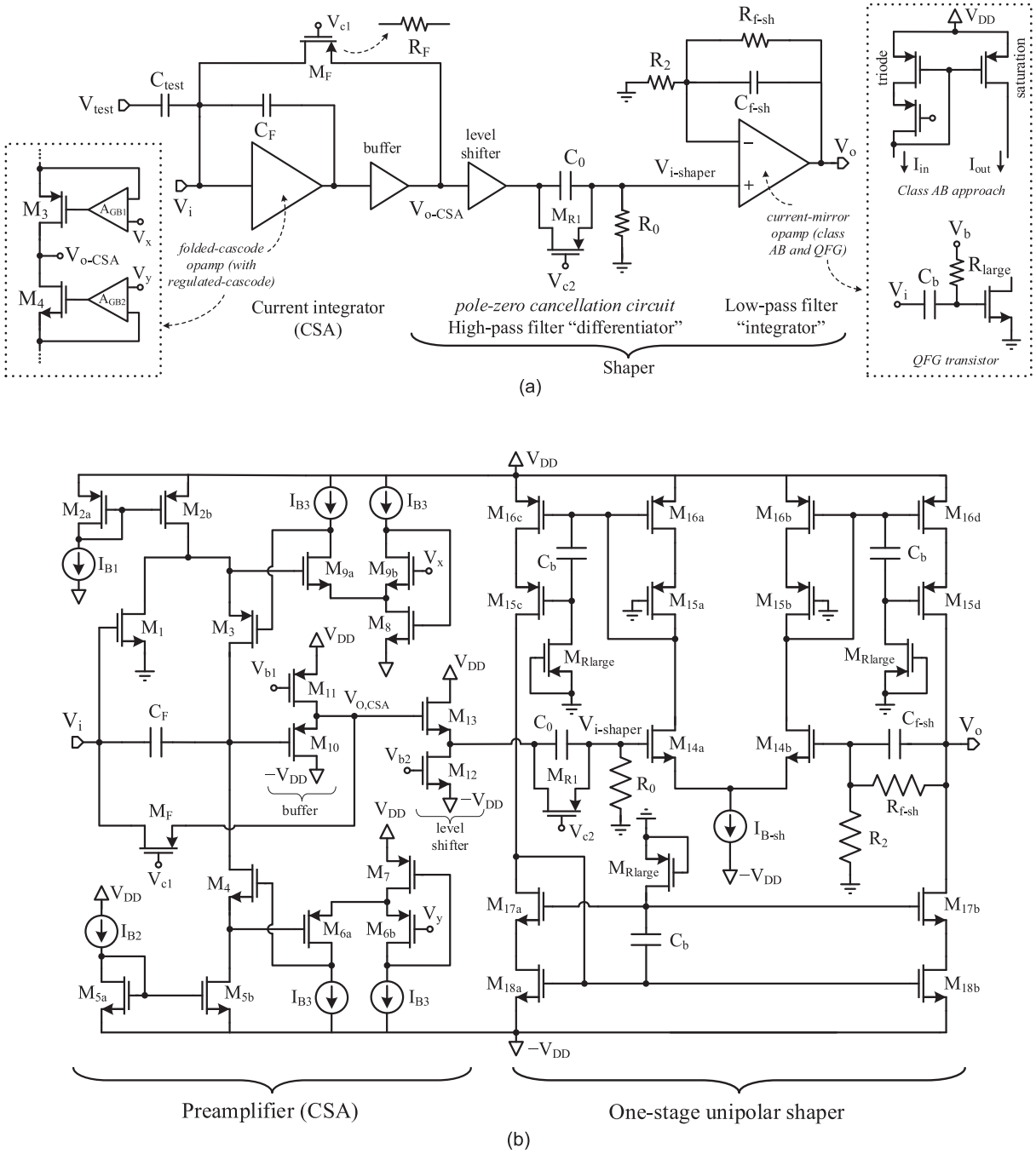



**Fig. 2.** Proposed front-end channel. (a) Building blocks. (b) Schematic of the circuit at transistor level.

### 3.1. Preamplifier

The CSA implementation is based on a folded-cascode structure composed of transistors $M_1$, $M_3$, $M_4$ and $M_5$. This topology provides a high gain together with a relatively large bandwidth [22,23]. While the input transistor of the folded-cascode is an nMOS, the cascode (or common-gate) transistor is a pMOS, which allows the DC levels of the input and output signals to be equal. In such a configuration, the parameters determining the open-loop gain are the ratio of the currents in the left and right branches of the folded-cascode, the dimensions of the input and load transistors, and the amount of current $I_{d1}$ flowing through the input transistor.

Regarding the reset mechanism of the CSA, the integrated element continuously discharges the feedback capacitance, provides a DC path for the leakage current of the detector, and defines the DC operating point of the amplifier. Although a simple resistor may seem to be a feasible reset device, its integration into a small silicon area is not possible. To avoid the use of a high-value resistance, a CSA reset circuit was implemented using a pMOS transistor ($M_F$) biased in the triode region.

The buffering of the output of the CSA, which is performed using transistors $M_{10}$ and $M_{11}$, provides the driving capability and the DC operating point of transistor $M_1$ through the feedback resistance $R_F$ ($M_F$). To couple the preamplifier with the shaper, a DC-level shifter was provided by the transistors $M_{12}$ and $M_{13}$. Biasing currents $I_{B1}$ and $I_{B2}$ are provided by transistors $M_2$ and $M_5$, which are implemented using a current source architecture.

For stability, a feedback capacitor ($C_F$) is placed between the CSA

input node and the gate of the source follower transistor configuration stage. The input node, which is connected to both $C_F$ and transistor $M_F$, discharges capacitance $C_F$.

The one-stage folded-cascode topology uses cascode transistors $M_3$ and $M_4$ to increase the output resistance (and gain), thereby achieving an accurate charge-to-voltage conversion for the preamplifier. The use of cascode transistors limit the output swing to $V_{DD}-(|V_{OD2b}|+|V_{OD3}|+V_{OD4}+V_{OD5b})$, where $V_{ODi}=V_{GSi}-V_{THi}$ denotes the overdrive voltage of $M_i$. Nevertheless, the output voltage of the CSA usually swings tens of millivolts, and it does preclude the use of cascode transistors.

The small-signal voltage gain is given by: $A_v = G_m \bullet r_{out}$, being $G_m \approx g_{m1}$, due to the output short-circuit current being approximately equal to the drain current of $M_1$ since the impedance seen looking into the source of $M_3$, that is, $(g_{m3}+g_{mb3})^{-1}||r_{o3}$, is typically lower than $r_{o1}\,||\,r_{o2b}$. The output resistance $r_{out}$ is given by:

$$r_{out} = \{[1+(g_{m3}+g_{mb3})r_{o3}](r_{o1}\|r_{o2b})+r_{o3}\}\|\{[1+(g_{m4}+g_{mb4})r_{o4}]r_{o5b} + r_{o4}\} \tag{10}$$

Thus, the small-signal voltage gain is approximately:

$$A_v = G_m r_{out} \approx g_{m1}\{[g_{m3}r_{o3}(r_{o1}\|r_{o2b})]\,\|\,[g_{m4}r_{o4}r_{o5b}]\} \tag{11}$$

The transconductance of the input transistor is maximized by using a wide nMOS and ensuring that the bias current of the input transistor is substantially larger than the bias current of the cascode transistors. The unity-gain frequency is given by $g_{m1}/C_L$, where $C_L$ is the load capacitance in the output node. The second pole is mainly associated to the *folding* point, i.e., the time constant introduced by the impedance and parasitic capacitances at the source of $M_3$. This impedance is approximately $1/(g_{m3}+g_{mb3})$, and the total capacitance at this node arises from $C_{GS3}$, $C_{SB3}$, $C_{DB1}$, $C_{GD1}$, $C_{GD2b}$ and $C_{DB2b}$. The relatively low transconductance of $M_3$, and the high contribution of $M_{2b}$ to the total parasitic capacitance given that it must be wide enough to carry the drain currents of both branches of the op-amp, suggests that a carefully design must be made taking into account the other key parameters of the CSA.

*Gain-boosting technique:* The limited gain of one-stage op-amps, accentuated by modern CMOS technologies where transistors have degraded analog properties, and the difficulties in using two-stage op-amps at high speeds have forced the proposal of new topologies. Thus, the presented design also uses a gain-boosting approach based on the regulated cascode technique [24,25] to further increase the output resistance without stacking more cascode transistors, which would reduce the output swing, and thus, the charge range in which the front-end is capable of linear processing. It is a negative local feedback loop formed by a gain stage ($A_{GB}$) around cascode transistors $M_3$ and $M_4$, which maintains a constant voltage at the sources of these transistors as shown in Fig. 2(a). These local gain stages drive the gate of $M_3$ and $M_4$, forcing the voltages $V_{s3}$ and $V_{s4}$ to be equal to $V_x$ and $V_y$, respectively. Thus, the use of this local feedback keeps stable the drain-source voltage across $M_{2b}$ and $M_{5b}$ in Fig. 2(b) against voltage variations at the drains of $M_3$ and $M_4$, yielding higher output resistance by a factor $(1+A_{GB})$.

The implementation of the local feedback amplifier is crucial to provide the desired enhanced output resistance without limiting the output swing, and with minimum additional waste of current. In this work, we have used a compact solution based on a common-source stage driven by transistor $M_{6a}$ (and its counterpart $M_{9a}$). The use of transistors $M_{6a}$ and $M_{9a}$ opposite in type from their cascode transistors does not decrease the output swing of the folded-cascode op-amp. The feedback loop also includes a flipped voltage follower (FVF) [26,27] formed by transistors $M_{6b}$, $M_7$ and $I_{B3}$. The connection between transistors $M_{6b}$ and $M_7$ provides a very low impedance node at the common source of $M_{6a}$ and $M_{6b}$ that sets the dc voltage at the drain of $M_{5b}$ to a value equal to the voltage $V_y$. The voltage at the sources of $M_{6a}$ and $M_{6b}$ can be considered constant due to the aforementioned very low resistance in this node that is given approximately by:

$$r_{FVF} \approx \frac{\frac{1}{g_{m6b}}\left(1+\frac{r_{o,IB3}}{r_{o6b}}\right)\|r_{o7}}{g_{m7}\left(r_{o6b}\|g_{m6b}r_{o6b}r_{o7}\right)} \tag{12}$$

As the source $I_{B3}$ is a simple current mirror ($r_{o,IB3}\approx r_{o6b}$), $r_{FVF}$ tends to $2/(g_{m6b}\bullet g_{m7}\bullet r_{o6b})$.

As the local feedback amplifier has a common source topology, its small-signal voltage gain can be approximated to $A_{GB2}\approx g_{m6a}\bullet r_{o6a}$ ($A_{GB1}\approx g_{m9a}\bullet r_{o9a}$). Therefore, the output resistance given in (10) is modified as follows:

$$r_{out} = \{[1+(g_{m3}+g_{mb3})r_{o3}(1+A_{GB1})](r_{o1}\|r_{o2b})+r_{o3}\}\| \{[1+(g_{m4}+g_{mb4})r_{o4}(1+A_{GB2})]r_{o5b}+r_{o4}\} \tag{13}$$

and the final voltage gain of the folded-cascode op-amp with gain-boosting shown in Fig. 2(b) is given by:

$$A_v = G_m r_{out} \approx g_{m1}[g_{m3}r_{o3}A_{GB1}(r_{o1}\|r_{2b})]\,\|\,[g_{m4}r_{o4}A_{GB2}r_{5b}] \tag{14}$$

To maintain $M_{6a}$ and $M_{9a}$ at saturation, the sizes of $M_{6a}$, $M_4$, $M_{9a}$ and $M_3$, and bias current $I_{B3}$ were carefully adjusted. To maximise $g_{m1}$: $g_{m1}=\sqrt{2\mu_n C_{ox}(W/L)I_{d1}}$, the bias current of $M_1$ is substantially larger than the bias current of the cascode transistors, also resulting in a higher $r_o$ for all transistors connected to the output branch of the folded-cascode op-amp: $r_o\ \alpha\ 1/(\lambda\bullet I_d)$, where $\lambda$ denotes the channel-length modulation coefficient.

Regarding the stability of each regulated cascode structure formed by $M_{6a}$, $M_{6b}$, and $M_7$ (and that formed by $M_8$, $M_{9a}$, $M_{9b}$), each contains two independent negative feedback loops. The first structure consists of $M_{6b}$ and $M_7$, with two poles: the dominant pole is located at the drain of $M_{6b}$ (high-impedance node) and is given by:

$$\omega_y = \frac{1}{R_y C_y} \approx \frac{1}{\left(r_{o,IB3}\|g_{m6b}r_{o6b}r_{o7}\right)C_y} \tag{15}$$

and the high-frequency pole is located at the source of $M_{6b}$ and is given by:

$$\omega_x = \frac{1}{R_x C_x} \approx \frac{1}{\left(\frac{1+r_{o,IB3}/r_{o6b}}{g_{m6b}}\|r_{o7}\right)C_x} \tag{16}$$

where $C_y$ and $C_x$ are the total capacitance at the aforementioned nodes. As the gain bandwidth product is given by $g_{m7}/C_y$, the stability is ensured if the condition $\omega_x > 2(g_{m7}/C_y)$ is met, which leads to $C_x/C_y < (g_{m6b}/4\bullet g_{m7})$ for the above mentioned condition $r_{o,IB3}\approx r_{o6b}$. A detailed stability analysis reported in [26] shows that if the parasitic capacitance at the source of $M_{6b}$ is low, the condition to ensure stability is easily achieved by adequately sizing transistors $M_{6b}$ and $M_7$.

The second feedback loop inside the regulated cascode structure, formed by $M_4$ and $M_{6a}$ also contains two poles: the high-impedance node

**Table 1**
Transistor dimensions and bias condition of the preamplifier.

| Transistor | W/L (μm/μm) | Bias condition | |
|---|---|---|---|
| $M_1$ | 125/0.36 | | |
| $M_{2a}$, $M_{2b}$ | 120/0.36 | | |
| $M_3$ | 130/0.36 | | |
| $M_4$ | 100/0.36 | $V_{DD}$ | 0.9 V |
| $M_{5a}$, $M_{5b}$ | 15/0.36 | $-V_{DD}$ | −0.9 V |
| $M_{6a}$, $M_{6b}$ | 0.25/0.7 | $I_{B1}$ | 1 mA |
| $M_7$ | 0.5/0.36 | $I_{B2}$ | 250 μA |
| $M_8$ | 0.25/0.7 | $I_{B3}$ | 5 μA |
| $M_{9a}$, $M_{9b}$ | 0.25/0.25 | $V_y$ | −600 mV |
| $M_{10}$ | 5/0.36 | $V_x$ | 550 mV |
| $M_{11}$ | 0.72/0.36 | $C_F$ | 650 fF |
| $M_{12}$ | 1.2/0.36 | | |
| $M_{13}$ | 9/0.18 | | |
| $M_F$ | 0.22/6 | | |

at the gate of $M_4$ sets the dominant pole, and the very low-impedance node at the source of $M_4$ is responsible for the non-dominant pole. Therefore, the bandwidth is not significantly reduced since the gate-source capacitance associated with the cascode transistor $M_4$ dominates the Miller capacitance in the gain stage $M_{6a}$. Selecting the proper dimensions for $M_4$ and $M_{6a}$ ensured stability. The same analysis was performed on samples $M_3$, $M_8$, $M_{9a}$, $M_{9b}$.

The transistor dimensions and biasing conditions of the preamplifier are listed in Table 1. The drain current of the input transistor is 750 μA, the bias current of the cascode output transistors is 250 μA, and each gain-boosting block consumes 10 μA. Thus, the CSA consumes 1.87 mW, including the buffer and level shifter.

### 3.2. Semi-Gaussian unipolar shaper with a PZC circuit

The next stage of the readout front-end system is the shaper circuit as shown in Fig. 2(a). Because shapers (filters) are typically active structures, a first-order CR-RC scheme was used to minimise the power overhead of the active filter and comply with the requirements of a low power budget and small die size for each readout channel. The CR-RC shaper provided a unipolar semi-Gaussian output pulse as discussed in section 2. Thus, the pulse shaper is basically a band-pass filter whose first section is formed by the differentiator $C_o$-$R_o$, which sets the duration of the pulse by introducing a decay time constant. The low-pass filter, which is the next circuit section, acts as an amplifier and integrator in a non-inverting configuration. It uses resistive and capacitive feedback ($R_{f\text{-}sh}$ and $C_{f\text{-}sh}$), increases the rise time, and limits the noise bandwidth. The ratio $R_{f\text{-}sh}/R_2$ gives the DC gain, and the common-mode voltage is zero. When the CSA output pulse with its long tail is fed into the CR-RC filter, the response at the shaper output is:

$$v_{outSH}(s) = \frac{Q_{in}}{C_F}\cdot\frac{1}{s+\frac{1}{C_F R_F}}\cdot\frac{s}{s+\frac{1}{C_0 R_0}}\cdot\frac{1}{sC_{f-sh}R_{f-sh}+1} \tag{17}$$

In the time domain the above pulse has a long negative undershoot, whose amplitude and width depend on the time constant $\tau_F = C_F \bullet R_F$ and its relation to the filter time constants $\tau_0$ and $\tau_{f\text{-}sh}$. The undershoot causes a negative baseline shift at the shaper output and the loss of the amplitude resolution of the system. The undershoot can be eliminated by applying a pole-zero cancellation (PZC) circuit included in the differentiator itself to cancel the CSA pole. By adding an extra resistor $R_{pz}$ ($M_{R1}$ in Fig. 2) in parallel to capacitor $C_0$ the pulse at the shaper output is given by

$$v_{outSH}(s) = \frac{Q_{in}}{C_F}\cdot\frac{1}{s+\frac{1}{C_0(R_{pz}\|R_0)}}\cdot\frac{s+\frac{1}{C_0 R_{pz}}}{s+\frac{1}{C_F R_F}}\cdot\frac{1}{sC_{f-sh}R_{f-sh}+1} \tag{18}$$

Thus, if the relation $C_F \bullet R_F(M_F) = C_0 \bullet R_{pz}(M_{R1})$ is fulfilled, the above equation can be rewritten as

$$v_{outSH}(s) = \frac{Q_{in}}{C_F}\cdot\frac{1}{s+\frac{1}{C_0(R_{pz}\|R_0)}}\cdot\frac{1}{sC_{f-sh}R_{f-sh}+1} \tag{19}$$

with the pole of the CSA being cancelled by the zero of the PZC circuit, and an undershoot at the shaper output being avoided [28]. The new time constant after the PZC is equal to $C_0 \bullet (R_{pz}||R_0)$ and it is smaller than $\tau_F$. Transistor $M_{R1}$ is composed of two transistors in parallel that have the same aspect ratio as transistor $M_F$ (implemented by two transistors in series), and the gates of both transistors are tied to the DC voltages $V_{c1}$ and $V_{c2}$.

Fig. 2(b) shows at transistor level the implementation of the active device of the shaper. A current mirror topology has been proposed for the operational amplifier with a class-AB output branch based on dynamic cascode biasing techniques using quasi-floating-gate transistors (QFG) [29]. The amplifier does not require a compensation capacitor owing to its one-stage topology.

A drawback of a simple current mirror amplifier is that it suffers from low open-loop voltage gain, approximately $(g_m \bullet r_o)/2$, where $g_m \bullet r_o$ denotes the intrinsic transistor gain. In modern deep-submicrometer CMOS technologies, the intrinsic gain is degraded to low values, resulting in poor accuracy because the latter parameter depends on the open-loop gain. The use of cascode transistors in the output helps to increase the output resistance and, thus, the open-loop voltage gain to approximately $(g_m \bullet r_o)^2/2$,

$$A_v = G_m r_{out} \approx g_{m14}\{[g_{m15}r_{o15}r_{o16}]\|[g_{m17}r_{o17}r_{o18}]\} \tag{20}$$

i.e., practically the same expression in (11) as that for the folded-cascode op-amp without the regulated cascode technique.

On the other hand, the need for a fast signal response with a low quiescent current cannot be satisfied by class-A topologies because the bias current provides the maximum output current. The class-AB approach overcomes this restriction, achieving a good slew-rate-quiescent current tradeoff because the output currents reach maximum values that are several orders of magnitude higher than the bias current. Nevertheless, if the circuit uses cascode transistors in the output branch, it makes the class-AB operation difficult and limits the output swing, as explained below. Fig. 3 shows this problem and a detail of the proposed circuit solution.

*Class-AB operation:* Current boosting is achieved in the output

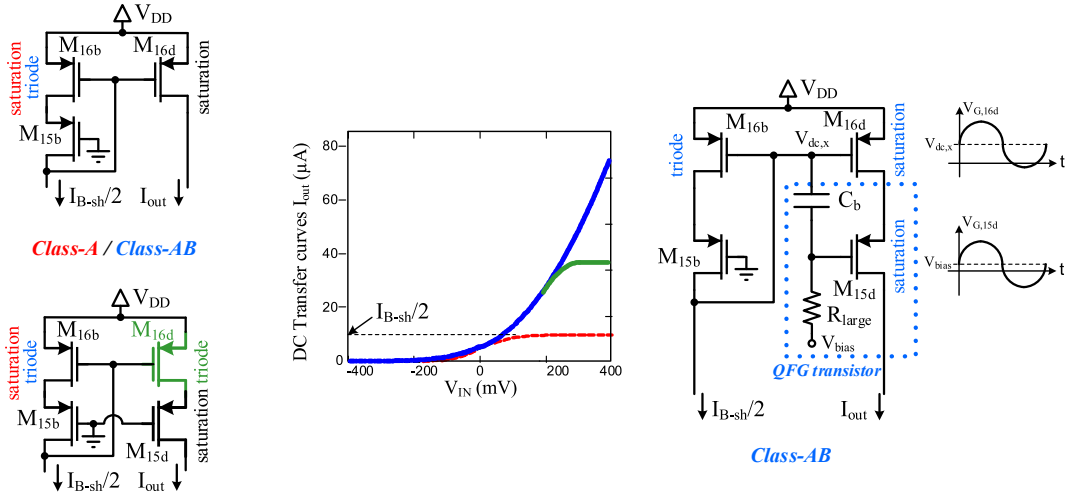



**Fig. 3.** Comparative between class-A and class-AB approaches, and proposed class-AB output based on the dynamic cascode biasing using QFG transistors.

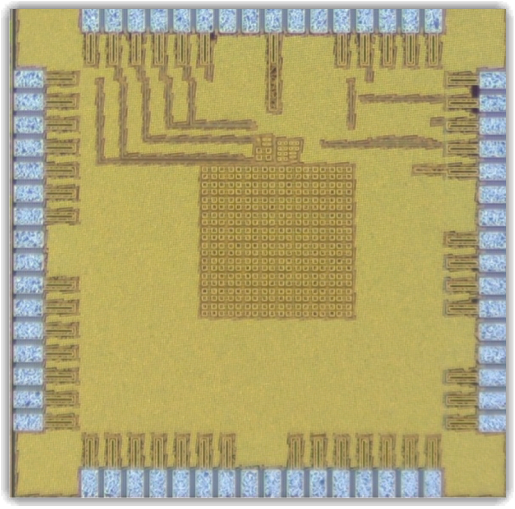
**Table 2**
Transistor dimensions and bias conditions of the shaper.

| Transistor | W/L (μm/μm) | Bias conditions | |
|---|---|---|---|
| $M_{14a}$, $M_{14b}$ | 2/0.36 | | |
| $M_{15a}$, $M_{15b}$, | 1.1/0.25 | | |
| $M_{15c}$ | 2.5/0.25 | $I_{B\text{-}sh}$ | 20 μA |
| $M_{15d}$ | 5/0.25 | $C_b$ | 1 pF |
| $M_{16a}$, $M_{16b}$, $M_{16c}$ | 1/0.25 | $C_0$ | 2.4 pF |
| $M_{16d}$ | 2/0.25 | $R_0$ | 15 kΩ |
| $M_{17a}$ | 2.5/0.36 | $C_{f\text{-}SH}$ | 300 fF |
| $M_{17b}$ | 0.36/0.36 | $R_{f\text{-}SH}$ | 150 kΩ |
| $M_{18a}$ | 5/0.36 | $R_2$ | 15 kΩ |
| $M_{18b}$ | 0.72/0.36 | | |
| $M_{R1}$ | 0.22/6 | | |
| $M_{Rlarge}$ | 50/0.18 | | |

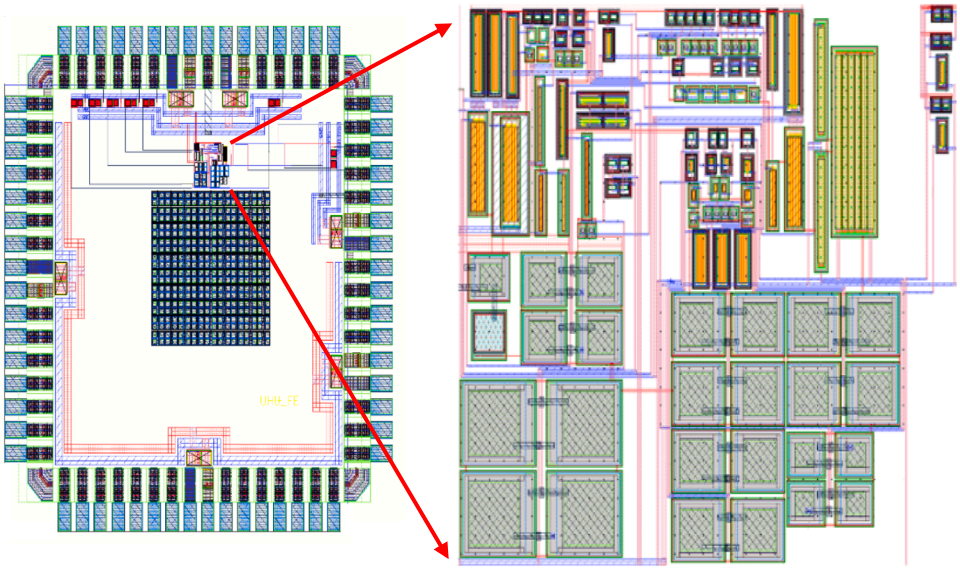
branches using an adaptive load formed by nonlinear current mirrors [30]. It operates as follows. The active load formed by transistor $M_{16}$ is a conventional current mirror, where all transistors operate in the saturation region under quiescent conditions, sinking the low current given by $I_{B\text{-}sh}/2$. However, $M_{16b}$ and its counterpart $M_{16a}$ (see Fig. 2b for transistors named with subscripts *a* and *c*) are biased near the triode region, with drain-source voltages $V_{DS}$ close to $V_{DS,sat}$. These $V_{DS}$ values were set based on $M_{15a}$ and $M_{15b}$ aspect ratios because their gates were tied to the ground, simplifying the design. With the input of the amplifier slew, the current increased, and the gate-to-source voltages of $M_{15a}$ and $M_{15b}$ also increased. This caused the transition of $M_{16a}$ and $M_{16b}$ from the saturation mode to the triode mode, featuring large gate

**Table 3**
Specifications of the ASIC.

| Parameter | Value |
|---|---|
| Fabrication process | TSMC 180 nm CMOS |
| Die size | 1.5 × 1.5 $mm^2$ |
| Active area | 0.028 $mm^2$ |
| Package | JLCC68 |
| Power supply | ±0.9 V |
| Power consumption | 1.97 mW |
| Detector / Sensor | 5 pF |



(a)



(b)

**Fig. 4.** (a) Microscope caption of the chip. (b). Layout.

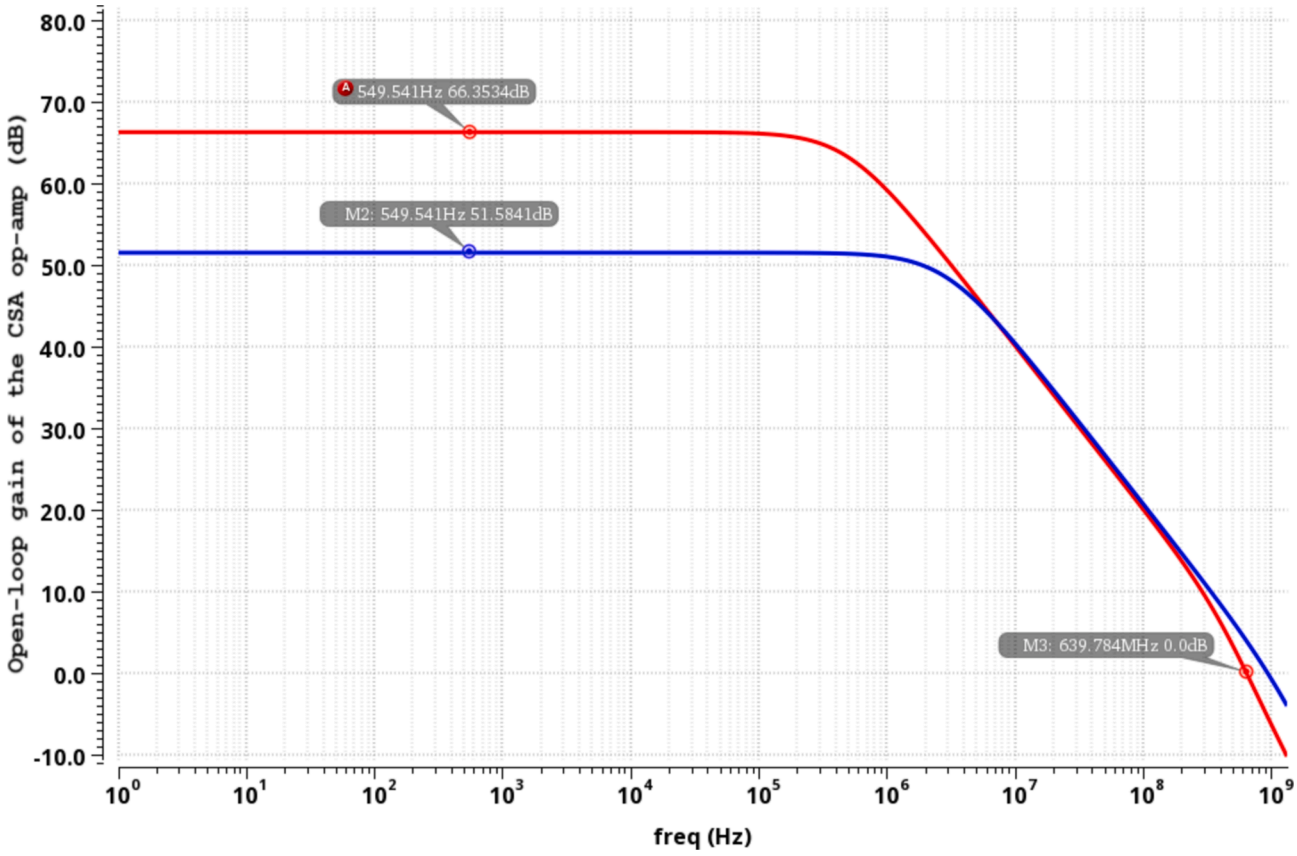



**Fig. 5.** Open-loop gain of the preamplifier with and without using the gain-boosting technique.

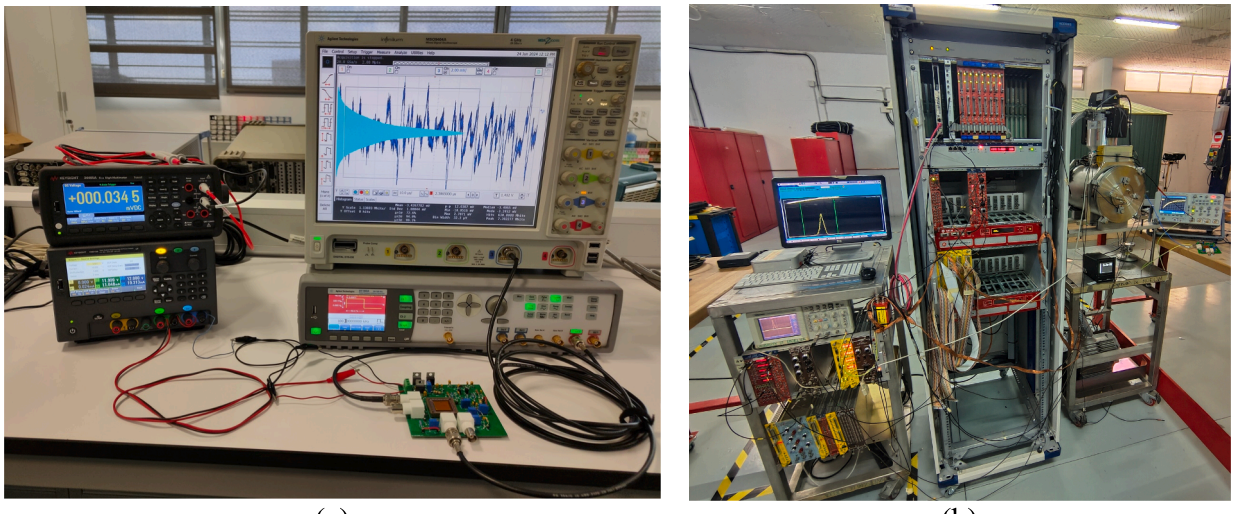



**Fig. 6.** Photographs of the test setup. (a) Electronics laboratory. (b) Nuclear technology laboratory.

voltage changes. Output current mirror transistors $M_{16c}$ and $M_{16d}$ remained in the saturation region, delivering larger output currents (quadratically) than the input currents provided by $M_{16a}$ and $M_{16b}$ as depicted in Fig. 3. Using the known expressions (neglecting second-order effects) for the drain current in the triode and saturation regions $I_D = K(V_{GS} - V_{TH}) \bullet V_{DS}$ and $I_D = (K/2)(V_{GS} - V_{TH})^2$, respectively, the nonlinearity of these current mirrors yields the desired output current boosting (class-AB behaviour) using the following expression:

$$I_{D,16d} = \frac{K_{16d}}{2}\left(\frac{I_{D,16b}}{K_{16b} \bullet V_{SD,16b}}\right)^2 \tag{21}$$

where $K_{16b,16d} = \mu \bullet C_{ox} \bullet (W/L)$ denotes the transconductance factor of transistors $M_{16b}$ and $M_{16d}$, and $V_{SD,16b}$ is set to $V_{SD,16b} = V_{DD} - \sqrt{I_{B-sh}/K_{15b}} + |V_{THP}|$. The analysis was similar for the other branches of the current mirror amplifier.

This current boosting typically precludes the use of cascode

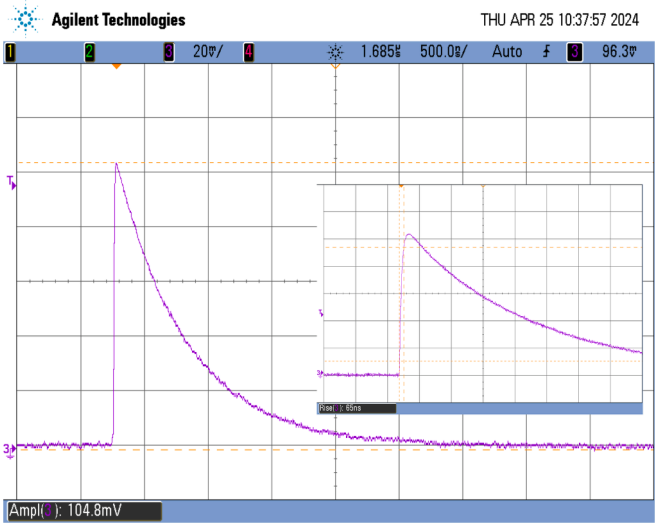



**Fig. 7.** Transient response of the preamplifier for a current input pulse of 1.5 MeV and rise time.

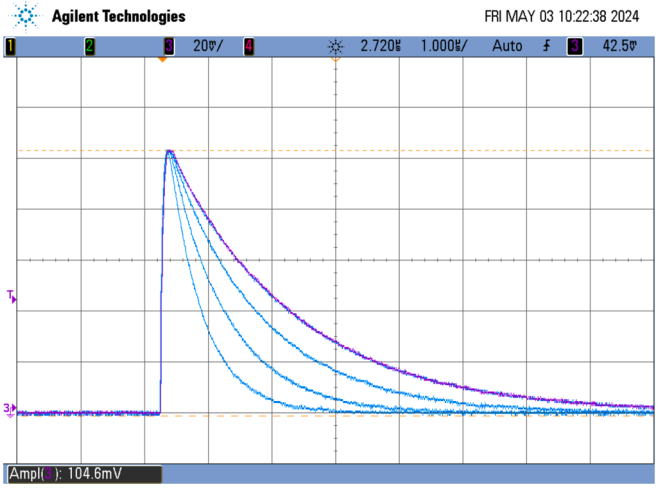



**Fig. 8.** Tunability of the decay time.

transistors in the output branch because if a classical cascode scheme is used, a large increase in the current causes an increase in the gate-source voltages ($M_{15c}$ and $M_{15d}$), driving $M_{16c}$ and $M_{16d}$ into the triode region, as shown at the bottom left of Fig. 3. Consequently, the slew rate enhancement factor was considerably reduced.

The solution is to adapt the gate voltage of cascode transistors $M_{15c}$, $M_{15d}$, $M_{17a}$ and $M_{17b}$ to their drain current. The quasi-floating gate technique developed by $R_{large}$ ($M_{Rlarge}$) and $C_b$ was used to provide a simple scheme without additional power consumption [31,32], as shown on the right side of Fig. 3. Transistors $M_{Rlarge}$ operate in the cutoff region and exhibit large resistances. Therefore, all cascode transistors have gates set to the ground under quiescent conditions as shown in Fig. 2b (in Fig. 3 it has been denoted $V_{bias}$ to highlight the operation of a QFG transistor). However, for dynamic operation, when the gates of triode transistors $M_{16a}$ and $M_{16b}$ feature a large change, these variations are also transferred to the gates of the cascode transistors by the capacitors $C_b$ and the large time constant of the quasi-floating gate RC networks ($C_b \bullet M_{Rlarge}$). This precludes the transistors $M_{16c}$ and $M_{16d}$ from entering the triode region; thus, they can deliver current boosting. The class-AB strategy was achieved without additional power consumption and with simplicity in the design.

Table 2 shows transistor dimensions and biasing conditions. The power consumption of the shaping circuit is 0.1 mW. Thus, the total power dissipation of the readout preamplifier-shaper channel is 1.97 mW.

## 4. Noise analysis

The design procedure for front-end electronic systems must consider noise optimisation. The noise performance of a detector readout system is generally expressed as the equivalent noise charge (ENC). The ENC corresponds to the charge that must be delivered to the front-end to achieve an output signal-to-noise ratio equal to unity. Although some parameters such as the detector capacitor, peaking time, and order of the shaping filter are related to the total noise, the main noise contributor is the preamplifier, where the ENC must be as low as possible to avoid degradation of the intrinsic detector energy resolution [33].

The total integrated rms noise at the output of the pulse shaper is given by

$$v_{total}^2 = \int_0^\infty |v_o(j\omega)|^2 |H(j\omega)|^2 df \tag{22}$$

where $H(j\omega)$ is the transfer function of the shaper and $v_o(j\omega)$ is the noise power spectrum at the preamplifier output. Considering the accepted assumption that the total system noise arises solely from the input transistor $M_1$ of the CSA if the input device has sufficient gain, the noise contribution of $M_1$ is dominated by the thermal noise of the channel and $1/f$ noise from the interfaces, according to the simplified expression:

$$v_o^2(j\omega) = \left|\frac{C_{in}}{C_F}\right|^2 v_{eq}^2 = \left|\frac{C_{in}}{C_F}\right|^2 \left(\frac{8}{3} k_B T \frac{1}{g_{m1}} + \frac{K_f}{C_{ox}^2 WL} \frac{1}{f}\right) \tag{23}$$

where $v_{eq}$ is the total equivalent noise voltage of the input transistor, $C_{in}$ is the total preamplifier input capacitance, $k_B$ denotes the Boltzmann constant, $T$ the temperature, and $K_f$ denotes an intrinsic process parameter for $1/f$ noise. The other parameters have their conventional meaning.

The transfer function of the semi-Gaussian pulse shaper consisting of one RC differentiator and one integrator is given by:

$$H(j\omega) = \left(\frac{j\omega \bullet \tau_{diff}}{1 + j\omega \bullet \tau_{diff}}\right)\left(\frac{A}{1 + j\omega \bullet \tau_{int}}\right) \tag{24}$$

where $\tau_{diff}$ and $\tau_{int}$ are the time constants of the differentiator and integrator, respectively, and $A$ is the dc gain of the integrator.

Substituting (23) and (24) in (22), and dividing to the signal amplitude due to one electron charge, the formulas for noise taking into consideration both thermal and flicker contributions are given by:

$$ENC_w^2 = \frac{8}{3} kT \frac{1}{g_{m1}} \frac{C_{in}^2 B\left(\frac{3}{2}, \frac{1}{2}\right)}{q^2 4\pi\tau_p} e^2 \tag{25}$$

$$ENC_f^2 = \frac{K_f}{C_{ox}^2 WL} \frac{C_{in}^2}{2q^2} e^2 \tag{26}$$

where $B$ is the function beta [34] that is 1.57 for one integrator, and $\tau_p$ is the peaking time of the shaper. For the mentioned value of $B$, (25) reduces to the classical expression for $ENC_w$: $ENC_w^2 \approx (k \bullet T \bullet C_{in}^2 \bullet e^2)/(2 \bullet g_{m1} \bullet q^2 \bullet \tau_p)$.

The flicker noise is inversely proportional to the gate area of the input transistor, strongly dependent on the technology process, and independent on the peaking time. For the relatively long-channel CMOS process used in this study (180 nm), the contribution of $1/f$ noise can be neglected, and the low peaking time (90 ns) also contributes to the thermal noise being dominant. Moreover, the input transistor $M_1$ of the gain-boosted folded-cascode topology is optimised for reducing the thermal noise by using a significantly high transconductance of 9.6 mA/V, and a non-minimum channel length. A careful design is required to

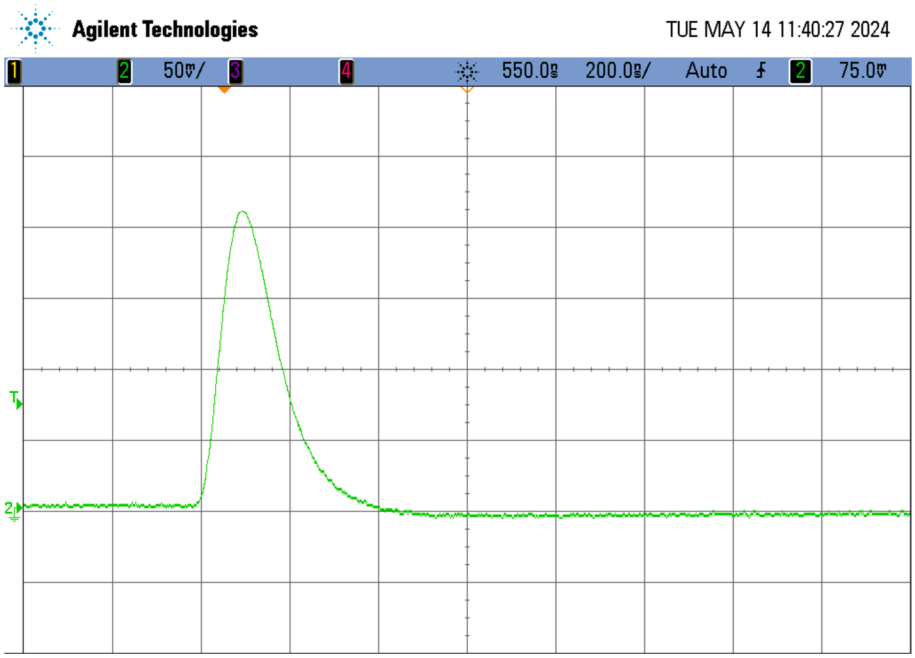



**Fig. 9.** Measured time response at the shaper output.

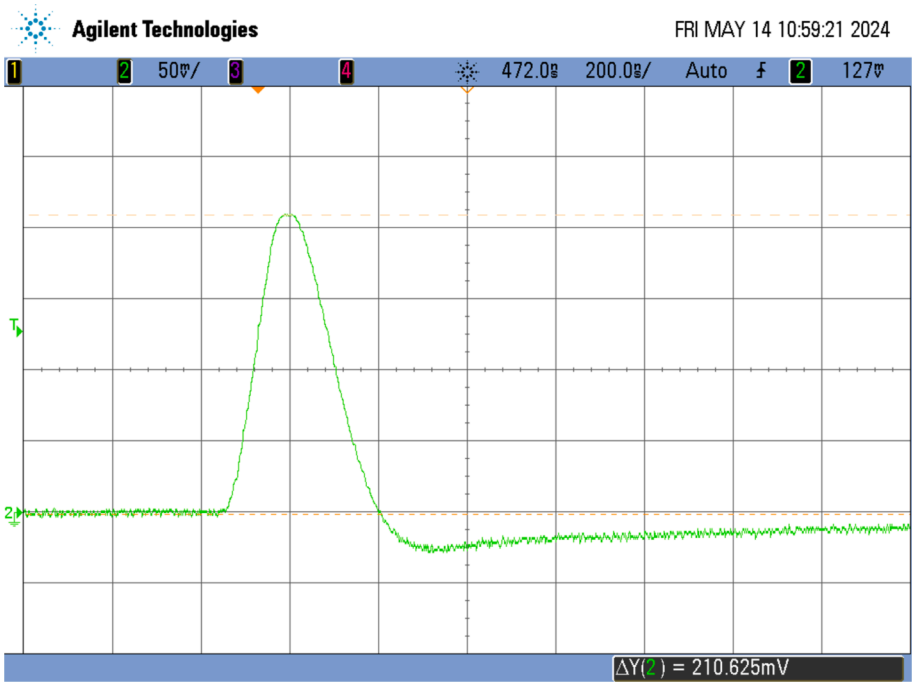


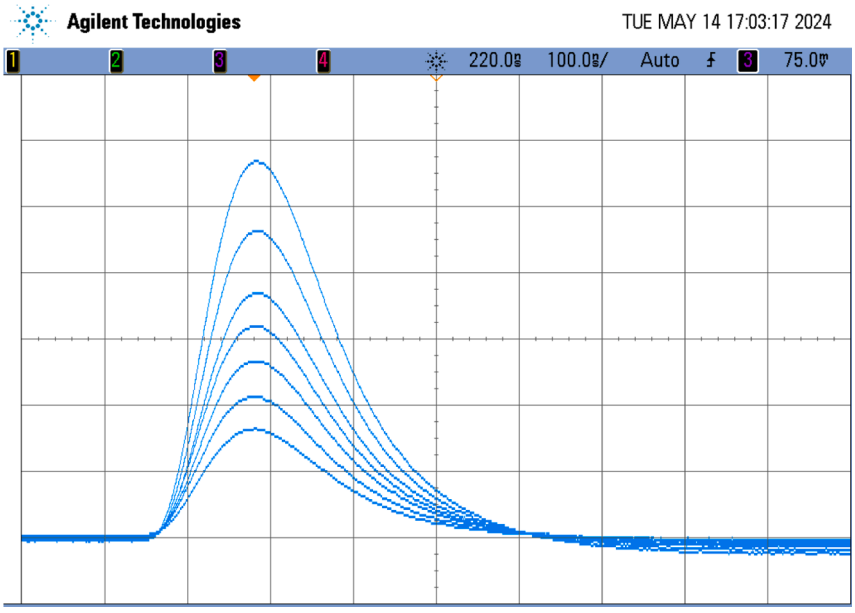

**Fig. 10.** Measured response at the shaper output for an inaccurate pole-zero cancellation.

minimise the contribution to the input noise from the transistors operating in the current sources ($M_{2b}$ and $M_{5b}$) in Fig. 2(b), resulting in $g_{m1} \gg g_{m2b}$, $g_{m5b}$. Subsequently, the output branch is optimised to achieve the required high gain.

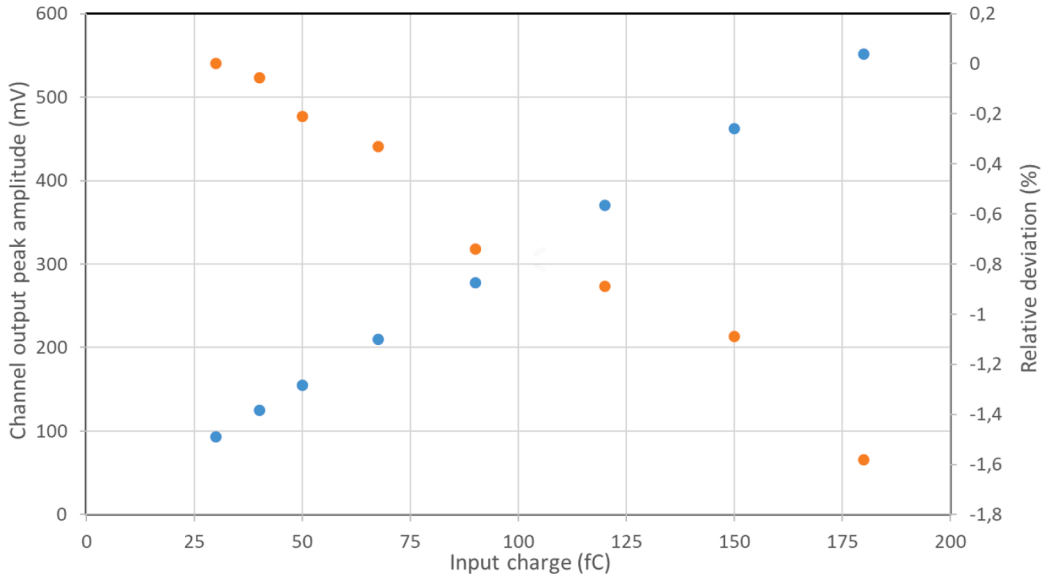
Advanced models of noise consider possible excess noise that may arise in submicron transistors owing to short channel effects [35], with equations and parameters that can be strongly dependent on the technology since modern CMOS technologies are developed for digital design. Other parameters such as, the inversion region (strong, moderate or weak) of the input transistor of the CSA, the noise associated with the detector leakage current, the detector bias resistance, and the effective feedback resistance $R_F$ in the CSA also contribute to the total noise.

## 5. Simulation and experimental results

The front-end channel has been designed, simulated, and fabricated in a TSMC 180 nm CMOS test chip prototype with power supplies of ±0.9 V. The microphotograph is shown in Fig. 4(a). The layout is also shown in Fig. 4(b) to clarify the image owing to the opaque passivation layer. The chip was packaged in a standard 68-pin J-leaded chip carrier (JLCC), and the active area is 176 μm × 157 μm = 0.028 $mm^2$. The chip specifications are listed in Table 3.




(a)




(b)

**Fig. 11.** (a) Output of the shaper for several input charge signals. (b) Output peak amplitude versus input charge and relative deviation.

Fig. 5 shows the open-loop frequency response of the preamplifier. A high open-loop gain was required to achieve an accurate charge-to-voltage conversion. Although the folded-cascode amplifier was a single-gain stage, its gain could be high because the product of the transconductance of the input transistor and the output resistance determine it. High transconductance is already required for noise and was maximised by using a wide nMOS device, and cascode techniques can achieve a significant output resistance. Moreover, as described previously, the bias current of the input transistor was considerably larger than that of the cascode transistors. This approach increased the transconductance and the output resistance ($r_o \approx 1/(\lambda \bullet I_d)$. As shown in Fig. 5, using the regulated cascode gain-boosting technique, a significantly high gain of 66 dB was achieved with a gain bandwidth product of 640 MHz (for a load capacitor of 1 pF), which meets the short-timing requirements. If this technique were not used, it can be noted that the gain decreases to 51 dB.

The system was measured using the calibrated pulse generator 81160A from Keysight to provide a square wave voltage signal of controlled amplitude. By applying a voltage step $V_{test}$ across an on-chip small test capacitor (Fig. 2a), a charge $Q_{in} = V_{test} \times C_{test}$ is injected into the input of the preamplifier. A high-speed time-domain digital oscilloscope is then used to analyze the characteristics of the FEE output pulse and measure the energy response. Fig. 6 shows photographs taken in the laboratories of electronics and nuclear technology of the Faculty of Experimental Sciences at the University of Huelva (Spain). It can be seen the printed circuit board with the chip prototype and the test instruments in Fig. 6(a). Fig. 6(b) shows the chamber containing the detector and other instruments commonly used in these experiments.

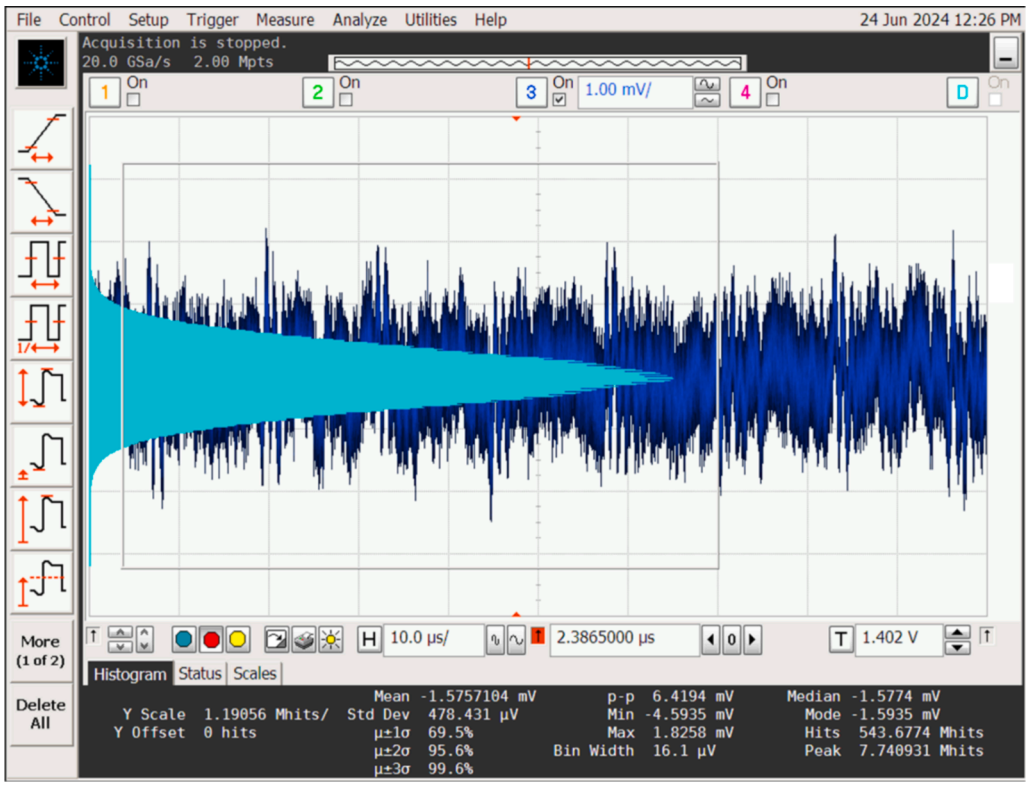



**Fig. 12.** An example of measured noise waveform and histogram of the readout channel.

Fig. 7 shows the output pulse of the preamplifier for an input charge of 67.5 fC, corresponding to the detection of approximately 1.5 MeV in silicon. The pulse height was about 104 mV (according to $v_{out} = (E \bullet 1.6 \bullet 10^{-19})/(\varepsilon \bullet C_F)$ in section 2), yielding a charge-to-voltage conversion rate of 1.54 mV/fC, and the rise time was 65 ns from 10 % to 90 % of the amplitude for an input capacitor of $C_{det} = 5$ pF.

The decay time is five times the time constant $R_F \cdot C_F$, and it can be programmed to meet the requirements of high-rate experiments. Fig. 8 shows this feature for estimated values of the active feedback resistance of 800 kΩ, 1.2 MΩ, 1.8 MΩ and 2.5 MΩ at several bias conditions of $M_F$.

Regarding the shaper, Fig. 9 shows the output pulse of the readout front-end channel to a 1.5 MeV charge signal, showing a peak height just above 210 mV, thus providing a pulse gain of 3.1 mV/fC. This low sensitivity is necessary to enlarge the input energy range that the system processes linearly because the output swing is limited owing to the use of cascode transistors in the output branch (both in the preamplifier and shaper). The peaking time, that is, the time required for the pulse to reach its maximum value, was approximately 90 ns.

Fig. 10 shows the undershoot in the shaper output when the pole of the preamplifier is not completely cancelled by the PZC circuit. Therefore, a change in the decay time of the preamplifier also influences the PZC network, which must be changed to preserve the same relationship and avoid an undershoot.

The output voltage of the readout channel should be linear within the detector charge range. Fig. 11(a) shows the shaper output at 90 ns shaping time for several charges injected at the input of the readout front-end, and Fig. 11(b) shows a nonlinearity of less than 1 % for up to 150 fC over this range. Finally, the readout front-end has been coupled to a silicon detector with a 5-pF capacitance, generating a measured ENC equal to 705 $e^-$, taking also into account the noise floor. Fig. 12 shows an example of noise histogram of the readout channel taken with the oscilloscope MSO9404A Infiniium 4 GHz from Keysight.

## 6. Conclusions

This paper presented the design of a readout front-end system in which the building blocks were based on one-stage amplifiers that employ gain-boosting and class-AB techniques to meet the required simplicity, power efficiency, and accuracy for modern front-end ASICs with several hundred channels used to measure the energy of charged particles in silicon detectors. The proposed circuit solutions preclude the degradation of the open-loop gain of the op-amps used in the readout channel in modern CMOS technologies without additional static power consumption. Thus, the charge-sensitive amplifier achieved an enhanced voltage gain of 15 dB, and the shaper consumed only 100 µW. The ASIC was fabricated using 180 nm complementary metal-oxide semiconductor technology. The measurement results confirm that the chip can process 30–150 fC of injected charge and is optimised for capacitance in approximately 5 pF.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgments

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## Data availability

No data was used for the research described in the article.

## References


[1] Rivetti A. CMOS front-end electronics for radiation sensors. CRC Press; 2015.
[2] Mansour M, Smith S, Kagan H, Caisley K, et al. A fast, low-jitter, and low-time-walk multi-channel front-end IC for diamond and silicon radiation detectors. IEEE Trans Nucl Sci 2023;70(7):1514–24.
[3] Tchamako AT, Ottaviani L, Rahajandraibe W, Vervisch W, Vervisch V, Walder JP. Front end electronics for radiation detectors based on SiC: Application to high dose per pulse charged particle beam current measurement. IEEE Sens J 2022;22(3): 2326–37.
[4] Sriskaran V, Alozy J, Ballabriga R, et al. New architecture for the analog front-end of Medipix4. Nucl Instrum Methods Phys Res A 2020;978:164412.
[5] Kmon P, Szczygieł R, Kleczek R, Górni D, Węgrzyn G, Niedzielska A, et al. Spectrum1k – integrated circuit for medical imaging designed in CMOS 40 nm. J Instrum 2022;17:C03023.
[6] Kwon I, Kang T, Wells BT, D'Aries LJ, Hammig MD. A high-gain 1.75-GHz dual-inductor transimpedance amplifier with gate noise suppression for fast radiation detection. IEEE Trans Circuits Syst II Exp Briefs 2016;63(4):356–60.
[7] Goyal SK, Naik AP. Design of low noise, high sensitive front end electronics for the charge readout from silicon photomultiplier detector for future space exploration programs. IEEE Int Symposium on Smart Electronic Systems (iSES) Ahmedabad, India 2023;2023:381–4.
[8] Romer M, Murray S, Schmitz J, Balkır S, Hoffman M. A low-power analog front-end amplifier for SiPM based radiation detectors. Nucl Instrum Methods Phys Res A 2023;1048:167897.
[9] Beikahmadi M, Mirabbasi S, Iniewski K. Design and analysis of a low-power readout circuit for CdZnTe detectors in 0.13-μm CMOS. IEEE Sens J 2015;16(4): 903–11.
[10] Kmon P, et al. Active feedback with leakage current compensation for charge sensitive amplifier used in hybrid pixel detector. IEEE Trans Nucl Sci 2019;66(3): 664–73.
[11] Schmitz JA, Rogge D, Balkir S, Hoffman MW, Bauer M. A low-power, highly integrated radiation detection system for portable, long-duration monitoring. IEEE Sens J 2020;20(18):10664–78.
[12] Kleczek R, Kmon P. Comparative analysis of the readout front-end electronics implemented in deep submicron technologies. J Instrum 2018;13:C11002.
[13] Beloso-Legarra J, De La Cruz-Blas CA, Lopez-Martin AJ. Power-efficient single-stage class-AB OTA based on non-linear nested current mirrors. IEEE Trans Circuits Syst I Regul Pap 2023;70(4):1566–79.
[14] Centurelli F, Della Sala R, Monsurró P, Tommasino P, Trifiletti A. An ultra-low-voltage class-AB OTA exploiting local CMFB and body-to-gate interface. AEU-Int J Electron 2022;145:154081.
[15] Ghorbanzadeh S, Dehbovid H, Ghorbani A, et al. Two-stage class-AB OTA with improved specifications. Analog Integr Circ Sig Process 2022;111:159–68.
[16] Nakhostin M. Signal processing for radiation detectors. John Wiley & Sons, Inc.; 2018.
[17] Galán J, López-Ahumada R, Sánchez-Rodríguez T, Torralba A, Carvajal RG, Martel I. Low voltage power efficient tunable shaper circuit with rail-to-rail output range for the HYDE detector at FAIR. IEEE Trans Nucl Sci 2014;61(2):844–51.
[18] Grybos P. Front-end electronics for multichannel semiconductor detector systems. Editorial Series on Accelerator Science. Institute of Electronic System, Warsaw University of Technology; 2010.
[19] Ohkawa S, Yoshizawa M, Husimi K. Direct synthesis of the Gaussian filter for nuclear pulse amplifiers. Nucl Inst Methods 1976;138:85–92.
[20] Soltveit HK, et al. The PreAmplifier ShAper for the ALICE TPC detector. Nucl Instrum Methods Phys Res A 2012;676:106–19.
[21] Liu F, Deng Z, He L, Liu Y. Development of the full-chain cryogenic readout electronics for the point-contact HPGe detectors. Nucl Instrum Methods Phys Res A 2019;947:162739.
[22] Gustavsson M, Amin FU, Björklid A, Ehliar A, Xu C, Svensson C. A high-rate energy-resolving photon-counting ASIC for spectral computed tomography. IEEE Trans Nucl Sci 2012;59(1):30–9.
[23] Perić I,, et al. High-voltage CMOS active pixel sensor. IEEE J Solid-State Circuits 2021;56(8):2488–502.
[24] Oliveira LB, Leitão CM, Medeiros SM. Noise performance of a regulated cascode transimpedance amplifier for radiation detectors. IEEE Trans Circuits Syst I Regul Pap 2012;59(9):1841–8.
[25] Vafaei M, Parhizgar A, Abiri E, Salehi MR. A low power and ultra-high input impedance analog front end based on fully differential difference inverter-based amplifier for biomedical applications. AEU-Int J Electron 2021;142:154005.
[26] Carvajal RG, Ramírez-Angulo J, Lopez-Martin AJ, Torralba A, Galan JA, Carlosena A, et al. The flipped voltage follower: A useful cell for low-voltage, low-power circuit design. IEEE Trans Circuits Syst I Regul Pap 2005;52(7):1276–91.
[27] Gupta OK, Pandey N, Gupta M. Improved frequency compensation technique of three stage amplifier using class AB flipped voltage follower and slew rate enhancer circuit. AEU-Int J Electron 2024;177:155173.
[28] Beikahmadi M, Iniewski K, Mirabbasi S. A low-power continuous-reset CMOS charge-sensitive amplifier for the readout of solid-state radiation detectors. *2016 14th IEEE International New Circuits and Systems Conference (NEWCAS)*, Vancouver, BC, Canada, 2016, pp. 1-4.
[29] Ramírez-Angulo J, López-Martín AJ, Carvajal RG, Chavero FM. Very low-voltage analog signal processing based on quasi-floating gate transistors. IEEE J Solid State Circuits 2004;39(3):434–42.
[30] Pedro M, et al. A linear compact tunable transconductor for Gm-C applications. Analog Integr Circ Sig Process 2012;72(2):351–61.
[31] Lujan-Martinez C, Hinojo-Montero J, Muñoz F, Rogelio-Palomo F, Martin-Holgado P, Morilla Y. Effect of ionizing radiation on quasi-floating gate transistors. AEU-Int J Electron 2023;170:154777.
[32] Sánchez-Rodríguez T, Gómez-Galán JA, Márquez F, Sánchez-Raya M, Hinojo J, Muñoz F. Analog CMOS readout channel for time and amplitude measurements with radiation sensitivity analysis for gain-boosting amplifiers. IEEE Access 2021;9: 148421–32.
[33] Noulis T, Siskos S, Sarrabayrouse G. Noise optimised charge-sensitive CMOS amplifier for capacitive radiation detectors. IET Circ Device Syst 2008;2(3): 324–34.
[34] Sansen WMC, Chang ZY. Limits of low noise performance of detector readout front ends in CMOS technology. IEEE Trans Circuits Syst 1990;37(11):1375–82.
[35] Ratti L, Manghisoni M, Re V, Traversi G. Design optimization of charge preamplifiers with CMOS processes in the 100 nm gate length regime. IEEE Trans Nucl Sci 2009;56(1):235–42.


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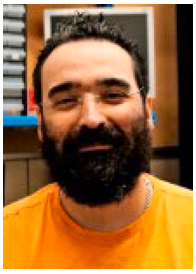

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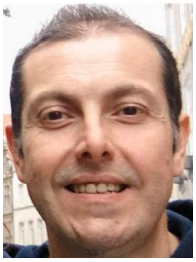

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