

## Article

# A Novel Transformerless Soft-Switching Symmetrical Bipolar Power Converter: Analysis, Design, Simulation and Validation

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**Abstract:** In order to obtain acceptable efficiencies, hard-switching techniques and the converters that implement them must operate at relatively low frequencies (tens of kilohertz), which translate into converters of large size, weight, and volume, and therefore higher cost. To improve these characteristics, this work introduces a new transformerless MHz-range DC–DC converter that provides symmetrical bipolar outputs. The developed topology uses a single grounded switch, achieves soft switching (ZVS) over a wide load range, and does not require the use of floating or isolated controllers, reducing cost, size, and complexity. The output voltages are self-regulated to maintain the same value, ensuring balanced bipolar operation. A comprehensive analysis, design, sizing, simulation, implementation and testing are provided on a 150 W prototype operating at a switching frequency of 1 MHz, with step-up and step-down capability and implemented with GaN FET. The evaluated configuration shows an efficiency close to 90% and high power density, making it suitable for compact designs in a variety of applications requiring reliable power management and high efficiency such as lighting, electric vehicles, or auxiliary power supplies.

**Keywords:** zero voltage switching (ZVS); soft-switching; high-frequency power converter; transformerless; GaN FET; bipolar output; symmetric outputs



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## 1. Introduction

The world's currently high demand for energy, combined with increasingly stringent regulations focused on sustainability and eco-friendly designs (ecodesign) [1–3], has created a strong need to optimize energy conversion systems. As industries seek more energy-efficient solutions, the integration of renewable sources and the development of advanced technologies become crucial. In this context, power converters, particularly DC–DC converters, play an essential role, being key components in a wide variety of industrial, consumer, and mobility applications, including electric vehicles and power management systems. These converters are responsible for adapting voltages in power conditioning systems, making the optimization of their operation critical for enhancing energy efficiency and achieving sustainable designs.

Traditionally, DC–DC converters employ hard-switching techniques to transfer power from the source to the load through controlled switches. However, this method is associated with two primary types of losses: conduction losses [4–6], due to the resistive components, and switching losses, which arise from the overlap of current and voltage during power semiconductor device switching [7–9]. Although the hard-switching method

has relatively fast transitions using power semiconductor devices, the switching process is not instantaneous, resulting in significant power dissipation, especially at high operating frequencies. To minimize these losses while maintaining high-frequency operation, which is necessary to reduce component size and maximize power density, alternative approaches are required.

To address these limitations, soft-switching techniques have emerged as a solution to reduce switching losses. By modifying the current or voltage waveform during switching transitions, soft-switching allows power losses to be minimized by ensuring that the voltage or current is near zero when the switch is activated. Resonant converters, which incorporate an  $LC$  resonant tank to smooth transitions, represent a significant advance over hard-switching. These converters can be further classified into quasi-resonant converters (QRC) and multi-resonant converters (MRC), depending on how many switches are associated with resonant circuits [10–14]. Moreover, quasi-resonant converters employ techniques such as zero voltage switching (ZVS) [15,16] or zero current switching (ZCS) [17,18] that allow for either voltage or current to be zero during switching, to increase frequency and optimize efficiency. Another classification is based on the way in which the resonant cycle is operated, distinguishing between full-wave and half-wave operation. In half-wave quasi-resonant converters, the internal diode of the power switch conducts during part of the cycle. In full-wave quasi-resonant converters, an extra diode is added to block this internal diode, allowing better control of the switching process. The full-wave configuration provides better load regulation compared to the half-wave counterpart, maintaining a nearly constant switching frequency despite load variations. However, the addition of an extra component increases cost and space requirements. This makes the full-wave converter more stable when the load changes, ensuring a more consistent operation, but assuming the addition of one additional diode.

In addition to these considerations, in applications where bipolar symmetric outputs are required, single-input bipolar symmetric output (SIBSO) and single-input multiple-output (SIMO) DC–DC converters have grown in relevance [19–21]. These converters are used in various applications, including lighting, auxiliary power supplies, and electric vehicle systems. Although traditional SIBSO converters are based on isolated transformers to generate bipolar outputs, these designs often suffer from inefficiencies and complexity due to the need for multiple controllers. However, transformerless SIBSO converters, which remove the need for isolation transformers, have emerged as a promising alternative, providing higher efficiency and power density. The use of new wide-bandgap semiconductors [22–26] like gallium nitride (GaN) field effect transistor (FET) [27,28] further enhances the efficiency of these converters by enabling high-frequency operation and reducing switching losses.

Furthermore, the implementation of wide-bandgap semiconductor devices such as GaN FET and Silicon Carbide (SiC) is transforming converter design. These materials allow for higher frequency operation with reduced switching losses, resulting in greater power density and efficiency. The combination of these technologies with soft-switching techniques presents a promising pathway toward the miniaturization and optimization of converters. As designs become more compact and efficient, electronic systems benefit from improved thermal management, lower cooling requirements, and increased reliability.

As technology advances and electrical applications become more complex, the demand for efficient and versatile power conversion solutions increases. The need for devices capable of handling multiple outputs and operating reliably under various conditions has led to special attention being focused on the development of power converters. SIBSO converters are not limited to conventional applications such as power supplies and audio systems but are also gaining acceptance in emerging areas like solar energy and electric

vehicles. In these contexts, the ability to generate symmetric outputs while maintaining high efficiency is critical to ensure optimal performance and economic viability of systems.

Moreover, it is essential to consider the impact that enhanced efficiency in DC–DC converters has on sustainability and the environment. As the transition toward renewable energy sources advances, the integration of efficient converters becomes crucial for maximizing the utilization of these sources. Well-designed converters not only reduce energy losses but also help decrease the carbon footprint of electrical systems. By promoting research and development of more sustainable energy conversion technologies, a precedent is set for the design of electrical systems that support a more efficient future.

This paper introduces a novel transformerless SIBSO DC–DC converter, utilizing GaN FET devices and soft-switching techniques to achieve high power density and efficiency. The proposed design incorporates just one gate-driven switch so that a single input can generate two bipolar outputs with common ground. The switch is grounded, eliminating the need for isolated sensors or drivers. ZVS is accomplished across the full load range, resulting in a more compact and cost-effective solution suitable for modern high-efficiency applications.

The rest of this paper is organized as follows: Sections 2 and 3 introduce the converter topology and describe and provide a theoretical study of the novel converter operating modes, including modeling and circuit behavior under different operating conditions. Section 4 details the component selection and practical considerations to develop the converter. Section 5 presents the simulation results that validate the analysis and illustrate the converter's performance. Section 6 develops a model to quantify losses, assessing overall efficiency. Section 7 presents measurements from the prototype, comparing them with theoretical and simulated results to validate the proper operation, and finally, Section 8 ends with conclusions.

## 2. Proposed Converter Topology

The proposed configuration consists of the combination of two quasi-resonant ZVS, full-wave, two-inductor converters, Cuk and SEPIC. Both topologies can be combined since they share the same front end. The SEPIC topology provides a positive output voltage, while the Cuk topology is used to obtain a negative output voltage, resulting in two bipolar, symmetrical or dual output voltages. This combination strategy has been described in [29], operating in hard-switching, while in [30,31], it was applied to similar topologies, operating in quasi-resonant half-wave version combination. The combination converter requires only one controllable power switch, which contributes to increasing the power density by using fewer components, being suited for converters up to some hundred watts and keeping continuous input and output currents. Another important advantage is that the proposed combined converter can operate in both step-down and step-up modes, increasing or decreasing the output voltage with respect to the voltage applied at its input. The two output voltages can be regulated by a single controller. There is a wide variety of applications in which converters with symmetrical or dual output (single-input dual-output, SIDO) are used [32]. The Cuk and SEPIC ZVS QR topologies are shown in Figures 1 and 2, respectively. Both are full-wave versions [12] for ZVS operation.

The new proposed configuration, resulting from the combination of Cuk and SEPIC, is shown in Figure 3, where the input inductor  $L_1$ , the power switch  $Q$  and the associated resonant circuit  $L_R$  and  $C_R$  are shared.

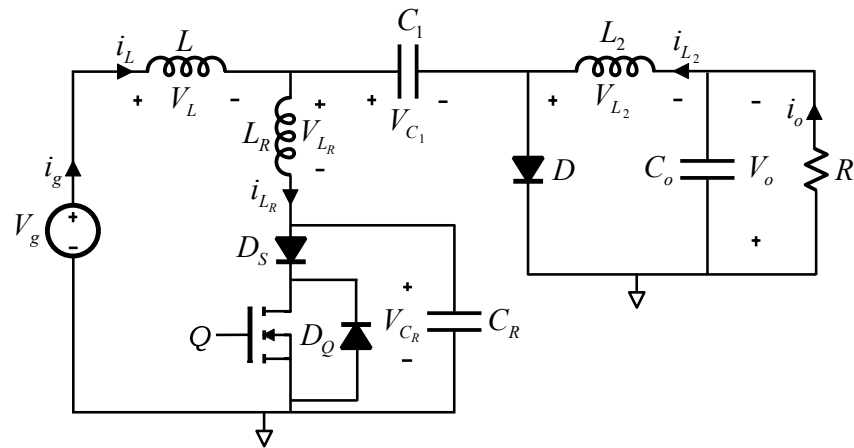


Figure 1. ZVS QR Cuk full-wave converter.

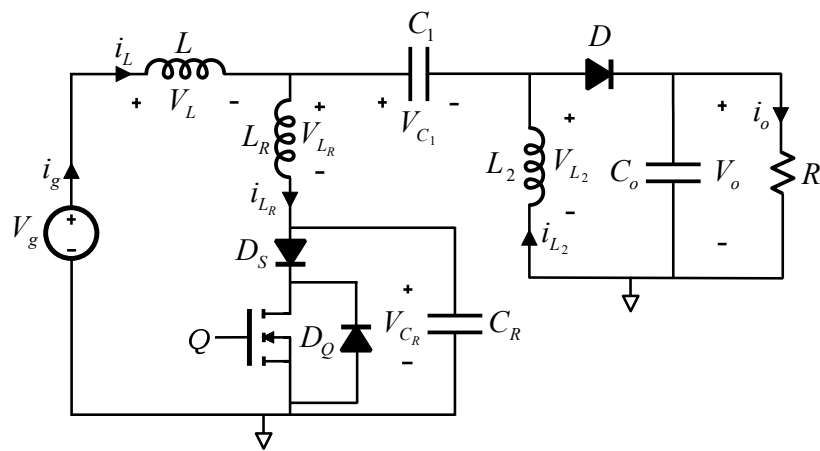


Figure 2. ZVS QR SEPIC full-wave converter.

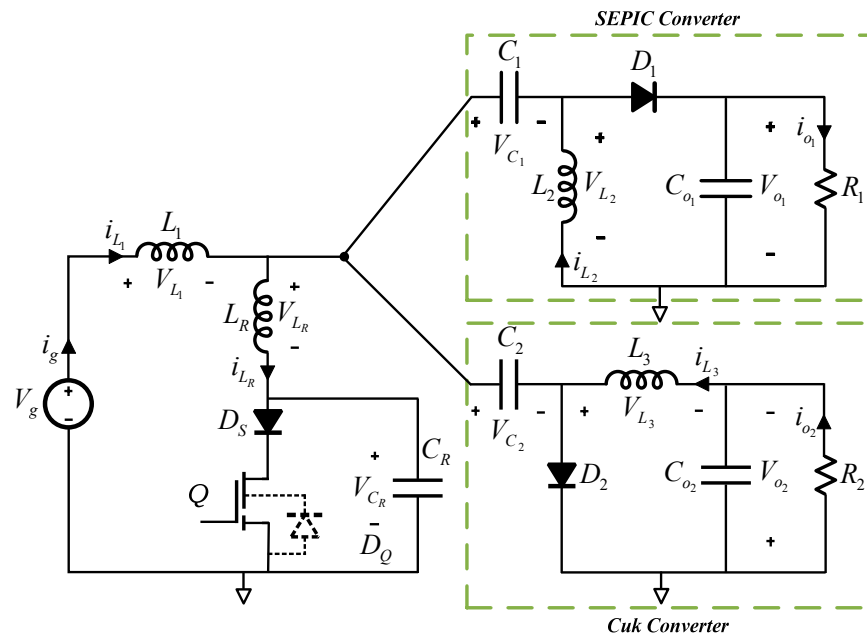


Figure 3. SIBSO ZVS QR Cuk-SEPIC combination converter.

The converter operates in four intervals. Initially, with  $Q$  and  $D_S$  off, the current from the filter inductor flows through the resonant tank ( $L_R$ - $C_R$ ), causing  $C_R$  to charge linearly. When  $C_R$  reaches the value of  $V_g + V_{o1}$  or  $V_g + V_{o2}$ ,  $D_1$  and  $D_2$  conduct, supplying

current to the loads while  $C_R$  follows a sinusoidal voltage variation. Once the resonant cycle completes and  $C_R$  returns to zero (at the end of the negative half-cycle),  $Q$  must be turned on to direct current through  $L_R$ , preventing further resonance. Finally,  $Q$  and  $D_S$  conduct while the freewheeling diodes turn off, restoring initial conditions before the next switching cycle begins, which will start when  $Q$  is turned off again.

### 3. Analysis of SIBSO ZVS QR Cuk–SEPIC and Operating Modes

The analysis of the ZVS QR Cuk–SEPIC full-wave combination converter (Figure 3) can be performed by dividing the period ( $T_s$ ) in four intervals, resulting in four equivalent circuits, showed in Figures 4–7. It is assumed that the currents through filter inductors ( $L_1, L_2$  and  $L_3$ ) and the capacitor ( $C_1, C_2, C_{o1}$  and  $C_{o2}$ ) voltages stay relatively constant during  $T_s$ .

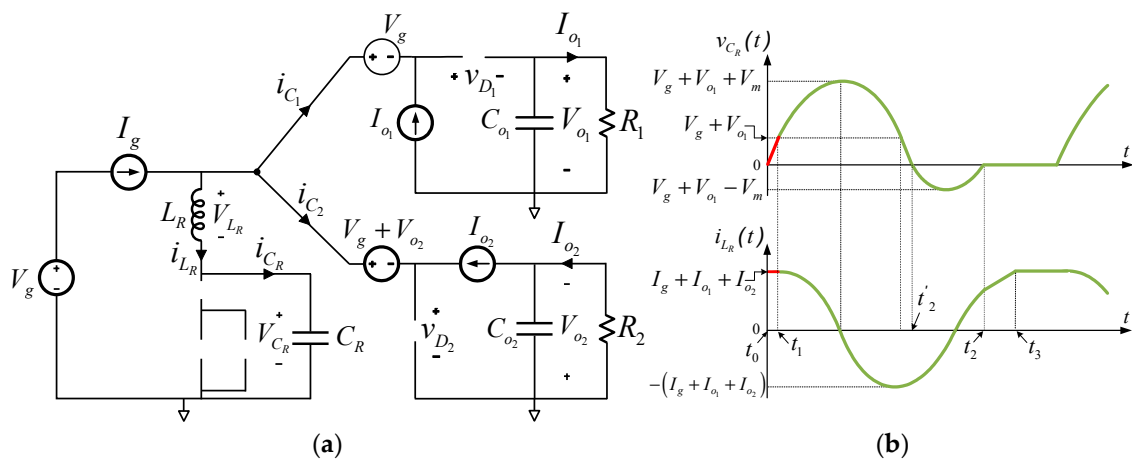
In addition, the following parameters (Equation (1)) and considerations are taken into account: semiconductors (diodes and GaN FET) are considered ideal (zero voltage drops, zero reverse currents, zero switching times and zero parasitic capacitors).

$$\begin{aligned} \text{Resonant Frequency (rad/s)} : \omega_0 &= 2\pi f_0 = \frac{1}{\sqrt{L_R \cdot C_R}} \\ \text{Characteristic Impedance (\Omega)} : Z_0 &= \sqrt{\frac{L_R}{C_R}} = \omega_0 \cdot L_R = \frac{1}{\omega_0 \cdot C_R} \end{aligned} \tag{1}$$

Assuming full-wave operation with respect to the resonant action,  $D_S$  does not allow conduction of the diode associated with the GaN FET ( $D_Q$ ), which causes the voltage across the resonant capacitor to change sign. The analysis begins by assuming the voltage across the resonant capacitor ( $C_R$ ) is zero (the power switch is turned on).

#### 1. Interval 1 (Linear stage) [ $t_1 - t_0$ ]:

At  $t_0$ ,  $Q$  and  $D_S$  are turned off (Figure 4). The currents of the filter inductors ( $L_1, L_2$  and  $L_3$ ) flow through  $L_R$  and  $C_R$ . The voltage at  $C_R$  (and thus also at  $Q$ ) grows linearly from zero (ZVS operation). This interval ends when  $C_R$  reaches the value of  $V_g + V_{o1}$  or  $V_g + V_{o2}$  and the free-wheeling diodes ( $D_1$  and  $D_2$ ) become directly biased ( $t_1$ ).



**Figure 4.** Linear stage. (a) Equivalent circuit of the ZVS QR Cuk–SEPIC full-wave combination converter during interval 1 [ $t_1 - t_0$ ]. (b) Main resonant waveforms (red: actual interval).

#### Analysis of Interval 1

The states of the power semiconductors are as follows:

$Q, D_Q, D_S, D_1$  and  $D_2$  off.

The initial conditions are as follows:

$$i_{L_R}(t_0) = i_{C_R}(t_0) = I_g + I_{o1} + I_{o2}, \quad v_{L_R}(t_0) = 0, \quad v_{C_R}(t_0) = 0$$

From circuit Kirchhoff laws, the following differential equations are obtained ( $t_1 - t_0$ ):

$$\begin{aligned}
 i_{L_R}(t) &= i_{C_R}(t) \text{ e } (I_g + I_{o1} + I_{o2}) = C_R \frac{dv_{C_R}}{dt} \\
 v_{C_R}(t) &= \frac{1}{C_R} \int_{t_0}^{t_1} i_{L_R}(t) dt \Rightarrow v_{C_R}(t_1) = v_{C_R}(0) + \frac{(I_g + I_{o1} + I_{o2})}{C_R} (t_1 - t_0) \\
 v_{C_R}(t_1) &= V_g + V_{o1} = V_g + V_{o2}
 \end{aligned}
 \tag{2}$$

The interval time duration is:

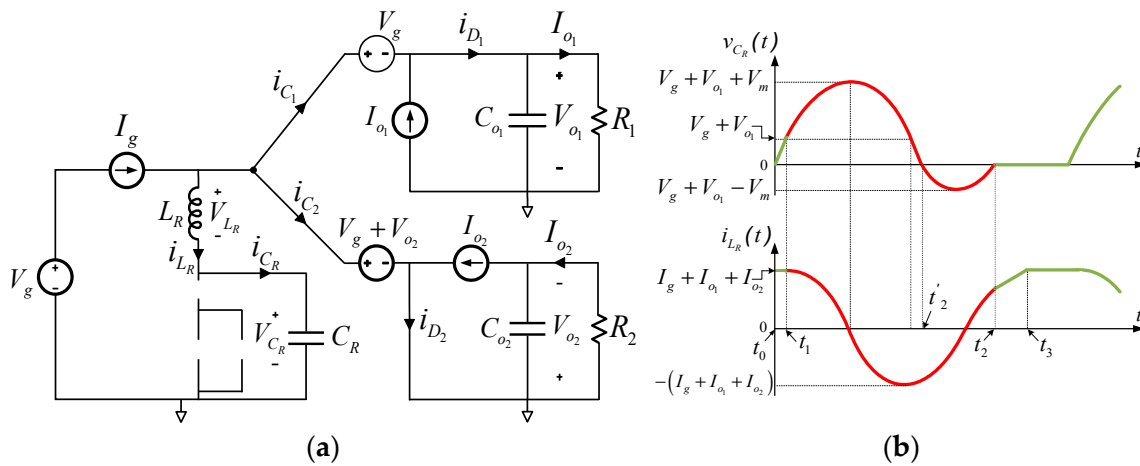
$$t_1 - t_0 = C_R \frac{(V_g + V_{o1})}{(I_g + I_{o1} + I_{o2})} = C_R \frac{(V_g + V_{o2})}{(I_g + I_{o1} + I_{o2})}$$

The diode voltages ( $D_1$  and  $D_2$ ) are as follows:

$$\begin{aligned}
 v_{D_1}(t) &= V_g + V_{o1} - v_{C_R}(t) = (V_g + V_{o1}) \left(1 - \frac{t-t_0}{t_1-t_0}\right) \\
 v_{D_2}(t) &= V_g + V_{o2} - v_{C_R}(t) = (V_g + V_{o2}) \left(1 - \frac{t-t_0}{t_1-t_0}\right)
 \end{aligned}
 \tag{3}$$

**2. Interval 2 (Resonant stage) [ $t_2 - t_1$ ]:**

At  $t_1$ , when  $C_R$  reaches the value of  $V_g + V_{o1}$ , diodes  $D_1$  and  $D_2$  are forward-biased and conduct the current to the loads (Figure 5). In this situation, the current flowing through  $C_R$  and  $L_R$  does not follow a linear evolution. The voltage across  $C_R$  varies sinusoidally, while the current through  $L_R$  varies cosenoidally. The maximum value in  $C_R$  reaches  $(V_g + V_{o1} + V_m)$  in the positive half-cycle, whereas the negative has a minimum value of  $(V_g + V_{o1} - V_m)$ . To analyze this evolution, the interval [ $t_2 - t_1$ ] is divided into two subintervals [ $t'_2 - t_1$ ] and [ $t_2 - t'_2$ ], delimited by each half-cycle of the resonant waveform.



**Figure 5.** Resonant stage. (a) Equivalent circuit of the ZVS QR Cuk–SEPIC full-wave combination converter during interval 2 [ $t_2 - t_1$ ]. (b) Main resonant waveforms (red: actual interval).

**Analysis of Interval 2:**

The states of the power semiconductors are as follows:

$Q, D_S$  and  $D_Q$  off.  $D_1$  and  $D_2$  on.

The initial conditions of the subinterval ( $t'_2 - t_1$ ) are as follows:

$$\begin{aligned}
 i_{L_R}(t_1) &= I_g + I_{o1} + I_{o2}, \quad v_{L_R}(t_1) = 0 \Rightarrow \frac{di_{L_R}}{dt}(t_1) = 0 \\
 v_{C_R}(t_1) &= V_g + V_{o1} \text{ and } i_{C_R}(t_1) = I_g + I_{o1} + I_{o2} \Rightarrow \frac{dv_{C_R}}{dt}(t_1) = \frac{I_g + I_{o1} + I_{o2}}{C_R}
 \end{aligned}$$

From circuit Kirchhoff laws, the following differential equations are obtained ( $t'_2 - t_1$ ):

$$\begin{aligned}
 i_{L_R}(t) &= i_{C_R}(t) \text{ and } V_g + V_{o1} = v_{C_R}(t) + v_{L_R}(t) \\
 \Rightarrow V_g + V_{o1} &= v_{C_R}(t) + L_R \frac{di_{L_R}}{dt} \xrightarrow{d/dt} 0 = \frac{i_{L_R}(t)}{C_R} + L_R \frac{d^2 i_{L_R}}{dt^2} \\
 \Rightarrow i_{L_R}(t) &= i_{C_R}(t) = (I_g + I_{o1} + I_{o2}) \cdot \cos[\omega_o(t - t_1)] \\
 \text{and } v_{C_R}(t) &= V_g + V_{o1} + (I_g + I_{o1} + I_{o2}) \cdot Z_o \cdot \sin[\omega_o(t - t_1)]
 \end{aligned} \tag{4}$$

At  $t'_2$  the voltage in  $C_R$  cross zero, thus:

$$t'_2 - t_1 = \frac{1}{\omega_o} \left( \sin^{-1} \left( \frac{(V_g + V_{o1})}{(I_g + I_{o1} + I_{o2}) \cdot Z_o} \right) + \pi \right)$$

Initial conditions of the subinterval ( $t_2 - t'_2$ ) are as follows:

$$i_{L_R}(t'_2) = (I_g + I_{o1} + I_{o2}) \cdot \cos[\omega_o(t'_2 - t_1)], v_{C_R}(t'_2) = 0 \text{ and } \frac{dv_{C_R}}{dt}(t'_2) = \frac{i_{L_R}(t'_2)}{C_R}$$

From circuit Kirchhoff laws, the following differential equations are obtained ( $t_2 - t'_2$ ):

$$\begin{aligned}
 i_{L_R}(t) &= i_{C_R}(t) \text{ and } V_g + V_{o1} = v_{C_R}(t) + v_{L_R}(t) \\
 \Rightarrow v_{C_R}(t) &= V_g + V_{o1} - L_R C_R \frac{d^2 v_{C_R}}{dt^2} \\
 v_{C_R}(t) &= (V_g + V_{o1})(1 - \cos[\omega_o(t - t'_2)]) + i_{L_R}(t'_2) Z_o \sin[\omega_o(t - t'_2)]
 \end{aligned} \tag{5}$$

At  $t_2$  the voltage in  $C_R$  reaches zero again:

$$t_2 - t'_2 = \frac{1}{\omega_o} \left( \sin^{-1} \left( \frac{2 \cdot (V_g + V_{o1}) \cdot i_{L_R}(t'_2) \cdot Z_o}{(V_g + V_{o1})^2 + i_{L_R}^2(t'_2) \cdot Z_o^2} \right) + \pi \right)$$

$$\begin{aligned}
 \text{While : } i_{D_1}(t) &= (I_g - i_{L_R}(t)) \left( \frac{R_2}{R_1 + R_2} \right) + I_{o1} \\
 \text{and } i_{D_2}(t) &= (I_g - i_{L_R}(t)) \left( \frac{R_1}{R_1 + R_2} \right) + I_{o2}
 \end{aligned}$$

3. Interval 3 (Discharge-inductor stage) [ $t_3 - t_2$ ]:

At  $t_2$ , the voltage in  $C_R$  reaches zero since the resonant full wave has been completed. Q must already be closed in order to conduct the current (together with  $D_S$ ) through  $L_R$  and prevent it from re-circulating through  $C_R$ , avoiding a repetition of the resonant wave (Figure 6). The interval will end when the free-wheeling diodes are turned off ( $t_3$ ).

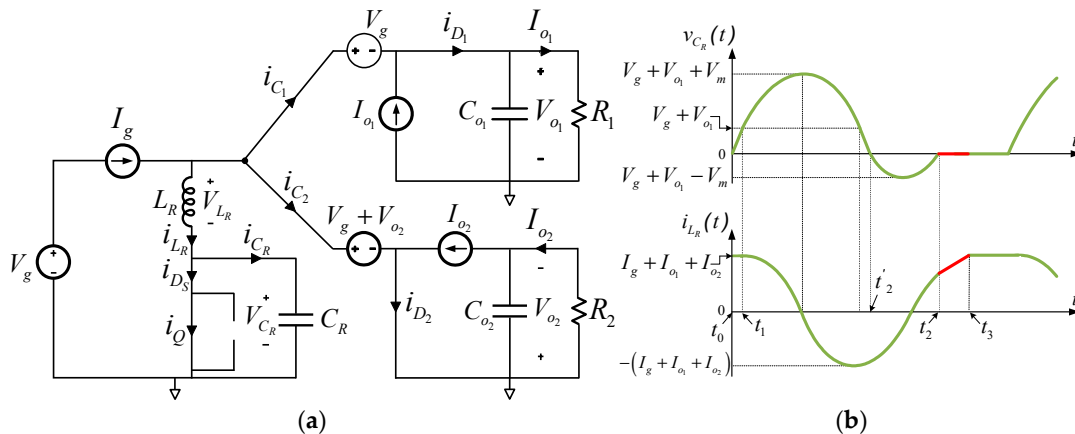


Figure 6. Discharge-inductor stage. (a) Equivalent circuit of the ZVS QR Cuk–SEPIC full-wave combination converter during interval 3 [ $t_3 - t_2$ ]. (b) Main resonant waveforms (red: actual interval).

**Analysis of Interval 3:**

The states of the power semiconductors are as follows:

$Q, D_S, D_1$  and  $D_2$  on.  $D_Q$  off.

The initial conditions are as follows:

$$i_{L_R}(t_2) = (I_g + I_{o1} + I_{o2}) \cdot \cos[\omega_o(t_2 - t_1)]$$

$$v_{L_R}(t_2) = V_g + V_{o1}, i_{C_R}(t_2) = 0 \text{ and } v_{C_R}(t_2) = 0$$

From circuit Kirchhoff laws, the following differential equations are obtained ( $t_3 - t_2$ ):

$$v_{L_R}(t) = V_g + V_{o1} \text{ y } v_{C_R}(t) = 0$$

$$\Rightarrow i_{L_R}(t) = \frac{1}{L_R} \int_{t_2}^{t_3} v_{L_R}(t) dt + i_{L_R}(t_2)$$

$$i_{L_R}(t_3) = \frac{1}{L_R} (V_g + V_{o1})(t_3 - t_2) + (I_g + I_{o1} + I_{o2}) \cdot \cos[\omega_o(t_2 - t_1)] \tag{6}$$

While :  $i_{D_1}(t) = (I_g - i_{L_R}(t)) \left( \frac{R_2}{R_1 + R_2} \right) + I_{o1}$

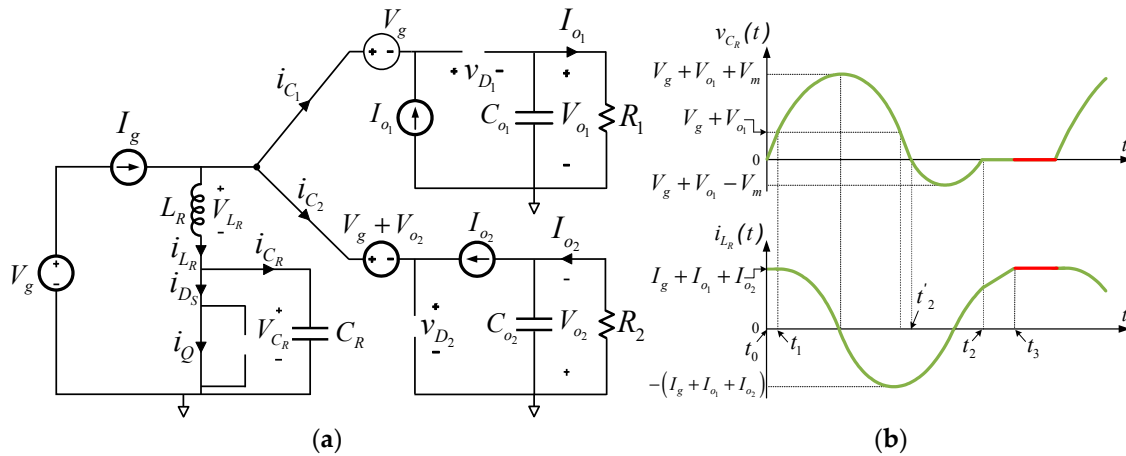
and  $i_{D_2}(t) = (I_g - i_{L_R}(t)) \left( \frac{R_1}{R_1 + R_2} \right) + I_{o2}$

The interval time duration is:

$$t_3 - t_2 = L_R \frac{(I_g + I_{o1} + I_{o2})}{(V_g + V_{o1})} [1 - \cos[\omega_o(t_2 - t_1)]]$$

**4. Interval 4 (Passive stage) [ $T_s - t_3$ ]:**

At  $t_3$ ,  $Q$  and  $D_S$  are in conduction, while the free-wheeling diodes are reverse-biased (Figure 7). All the variables reach their initial values for the following period. This interval ends when  $Q$  is turned off, therefore starting a new switching cycle.



**Figure 7.** Passive stage. (a) Equivalent circuit of the ZVS QR Cuk-SEPIC full-wave combination converter during interval 4 [ $T_s - t_3$ ]. (b) Main resonant waveforms (red: actual interval).

**Analysis of Interval 4:**

The states of the power semiconductors are as follows:

$Q, D_S$ , on.  $D_1, D_2$  and  $D_Q$  off.

The initial conditions are as follows:

$$i_{L_R}(t) = I_g + I_{o1} + I_{o2}, v_{L_R}(t) = 0, i_{C_R}(t) = 0 \text{ and } v_{C_R}(t) = 0$$

Figure 8 shows the main waveforms of the proposed converter, as well as their peak values, obtained in the previous analysis. The two symmetrical output voltages can be obtained by considering the average voltage at the free-wheeling diodes ( $D_1$  and  $D_2$ ) during a period, since these voltages are filtered by the output capacitors ( $C_{o1}$  and  $C_{o2}$ ).

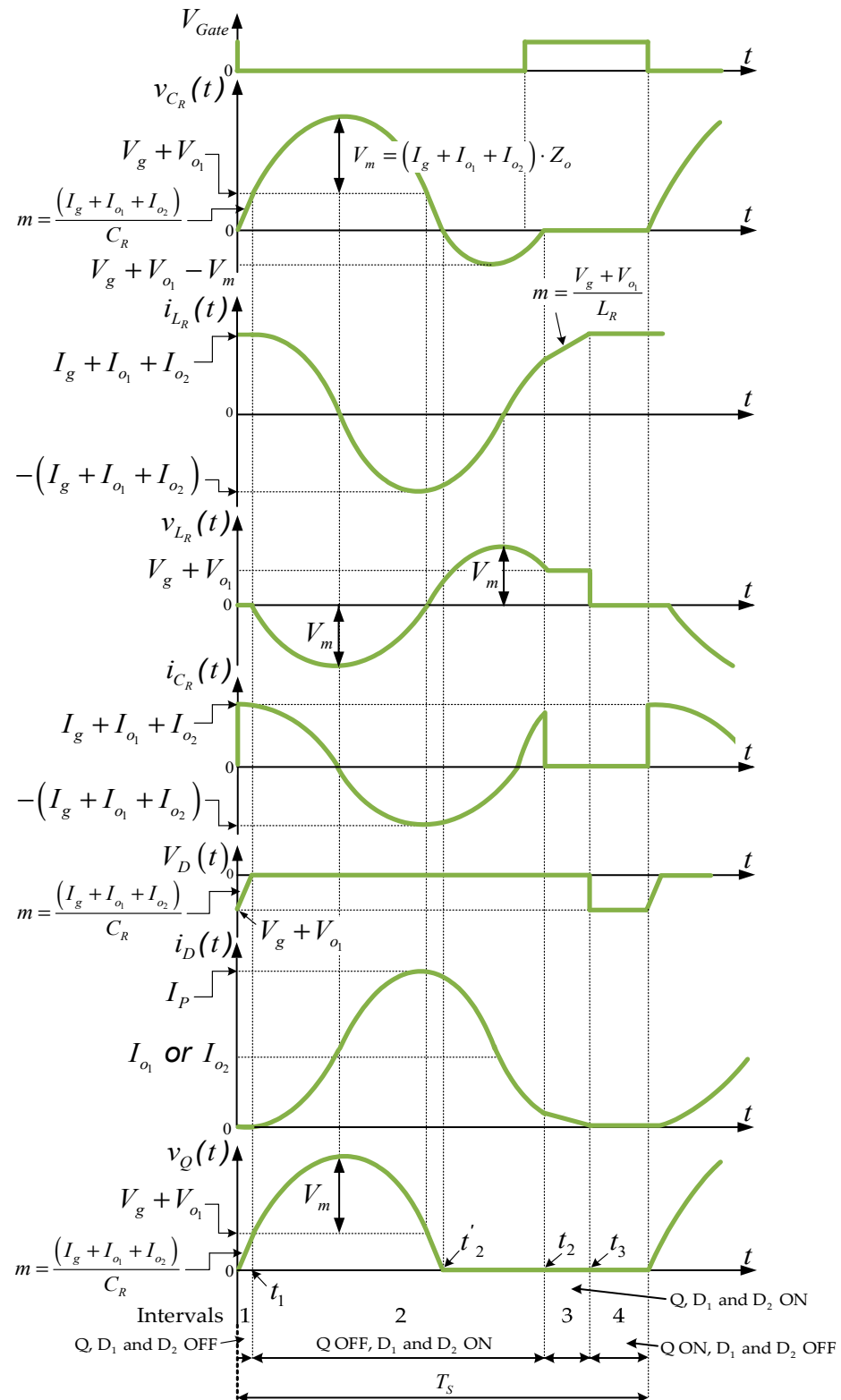


Figure 8. Main waveforms of the ZVS QR Cuk-SEPIC full-wave combination converter during the operating period.

The  $V_{D1}(t)$   $V_{D2}(t)$  voltages are given as:

$$V_{D1}(t) \text{ and } V_{D2}(t) = \begin{cases} \left[ -(V_g + V_{o1}) + \frac{(I_g + I_{o1} + I_{o2})}{C_R} (t - t_1) \right] & t_0 \leq t \leq t_1 \\ 0 & t_1 \leq t \leq t_2 \\ 0 & t_2 \leq t \leq t_3 \\ -(V_g + V_{o1}) & T_S \leq t \leq t_3 \end{cases}$$

The output voltages  $V_{o1}$  and  $V_{o2}$  are :  $\left. \begin{matrix} V_{o1} = |V_{D1}(t)_{AVG}| \\ V_{o2} = |V_{D2}(t)_{AVG}| \end{matrix} \right\}$

$$V_{o1} = V_{o2} = \frac{1}{T_s} \int_{t_0}^{t_2} \left[ (V_g + V_{o1}) - \frac{(I_g + I_{o1} + I_{o2})}{C_R} (t - t_1) \right] dt + \frac{1}{T_s} \int_{t_3}^{t_4} (V_g + V_{o1}) dt$$

And are given as:

$$\begin{aligned} V_{o1} = V_{o2} &= (V_g + V_{o1}) \left[ 1 - \frac{1}{T_s} \left( t_3 - \frac{t_1}{2} \right) \right] \Rightarrow V_{o1} = V_{o2} = V_g \cdot \frac{(1 - f_s \cdot (t_3 - \frac{t_1}{2}))}{f_s \cdot (t_3 - \frac{t_1}{2})} \\ \Rightarrow V_{o1} = V_{o2} &= V_g \cdot \frac{(1 - f_s \cdot (t_3 - \frac{t_1}{2}))}{f_s \cdot (t_3 - \frac{t_1}{2})} \end{aligned} \tag{7}$$

The current conversion relations can be expressed as:

$$I_g = (I_{o1} + I_{o2}) \cdot \frac{(1 - f_s \cdot (t_3 - \frac{t_1}{2}))}{f_s \cdot (t_3 - \frac{t_1}{2})} \tag{8}$$

Also, those conversion relations can be expressed by defining the parameter  $m$  as:

$$\begin{aligned} V_{o1} = V_{o2} &= V_g \cdot \frac{(1-m)}{m} \text{ and } I_g = (I_{o1} + I_{o2}) \cdot \frac{(1-m)}{m} \\ \text{With } m &= f_s \cdot \left( t_3 - \frac{t_1}{2} \right); 0 < m < 1 \end{aligned} \tag{9}$$

#### 4. Design and Sizing of the Combined SIBSO Converter

##### 4.1. Resonant Tank Selection

The design of the resonant tank begins by identifying the switching frequency required for operation. This value is fundamental, as it defines the dynamic behavior and maximum efficiency of the resonant converter. Considering that the resonant voltage must be greater than the input and output voltages combined for resonant action to be produced, the resonant inductor  $L_R$  is selected first, given its critical role in determining the tank's impedance.

The inductor value directly influences the efficiency of the converter; smaller inductances reduce the equivalent series resistance (ESR), minimizing conduction losses. However, the selection of  $L_R$  is bounded by the load impedance, as a smaller  $L_R$  decreases the tank's impedance. For effective resonant operation, the following condition must be satisfied:

$$V_{max, C_R} > V_g + V_o$$

where  $V_{max, C_R}$  is the maximum value of the voltage in the resonant capacitor. This ensures the resonant tank can sustain oscillatory energy exchange between  $L_R$  and  $C_R$ .

$$V_{max, C_R} = V_m = (I_g + I_{o1} + I_{o2}) \cdot Z_o$$

$$(I_g + I_{o1} + I_{o2}) \cdot Z_o > V_g + V_o; Z_o > \frac{V_g + V_{o1}}{I_g + \frac{V_{o1}}{R_1} + \frac{V_{o2}}{R_2}}; \sqrt{\frac{L_R}{C_R}} > \frac{V_g + V_{o1}}{I_g + \frac{V_{o1}}{R_1} + \frac{V_{o2}}{R_2}}$$

Once  $L_R$  is fixed, the resonant capacitor  $C_R$  is calculated using the resonant frequency definition (Equation (1)):

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{L_R \cdot C_R}}; m = \frac{1}{\frac{V_o}{V_g} + 1} = \frac{f_s}{f_o}$$

$$C_R = \frac{V_g^2}{L_R \cdot (V_g + V_o)^2 \cdot (2\pi \cdot f_s)^2} \text{ or } C_R = \frac{m^2}{L_R \cdot (2\pi \cdot f_s)^2}$$

For instance, with a switching frequency of 1 MHz, a standardized  $L_R$  value of 2.2  $\mu\text{H}$  and a required conversion ratio  $V_o/V_g = 24/48$  V, the calculated  $C_R$  is approximately 5.12 nF. In this design, a 4.7 nF standard capacitor was used, which resulted in a slight adjustment of the switching frequency to 1.044 MHz. This approach emphasizes the trade-off between using standardized components and fine-tuning operating parameters to achieve desired performance.

#### 4.1.1. Resonant Inductor

The sinusoidal nature of resonant tank currents introduces higher RMS currents, which amplify conduction losses. Selecting a resonant inductor with minimal ESR is critical to maintaining high efficiency. At high frequencies, additional considerations such as core losses, skin effect, and proximity effect become significant:

##### 1. Core Losses:

Ferromagnetic losses primarily consist of eddy current losses and hysteresis losses, both of which depend on the core material properties (Equation (10)). Their magnitude is influenced by the quadratic dependence on operating frequency and the magnetic flux density:

$$P_{core} = P_{eddy} + P_{hyst} = K_e \cdot f_s^2 \cdot B_{max}^2 \cdot t^2 \cdot V_{core} + K_h \cdot f_s \cdot B_{max}^\beta \cdot V_{core} \quad (10)$$

where

$K_e$ : Eddy current constant.

$B$ : Flux density.

$t$ : Material thickness.

$V$ : Volume.

$f_s$ : Switching frequency.

$K_h$ : Material coefficient.

**Core materials**, such as ferrites, exhibit losses due to hysteresis and eddy currents. At 1 MHz, these losses are significant, even for high-performance cores.

**Air-core inductors** completely eliminate core losses, making them ideal for high-frequency applications where relatively low inductance is required. However, the copper losses tend to be higher, as the air permeability is much lower.

##### 2. Skin Effect:

The skin effect reduces the effective section area of the conductor as the operating frequency increases. The penetration depth  $\delta$  is given by:

$$\delta = \sqrt{\frac{2 \cdot \rho}{\mu \cdot 2\pi \cdot f_s}}$$

where

$\mu$ : Magnetic permeability of the conductor.

$\rho$ : Electrical resistivity of the conductor.

For a copper wire operating at 1 MHz, the skin depth  $\delta$  is 65.23  $\mu\text{m}$ . Since only this thin outer layer conducts the current, the effective resistance increases, which increases losses.

### 3. Proximity Effect:

In multi-turn inductors, adjacent conductors induce opposing magnetic fields, further increasing effective resistance.

To mitigate some of these effects, designs should use the following:

**Litz wire:** Consisting of many thin, insulated strands to reduce skin and proximity effects.

**Flat or ribbon conductors:** To maximize the effective surface area and minimize resistance.

**Air core inductors:** Eliminating core losses and avoiding additional resistance introduced by magnetic materials.

#### 4.1.2. Resonant Capacitor

The resonant capacitor  $C_R$  must handle elevated RMS currents, which lead to conduction losses proportional to its ESR. Capacitor selection for high-frequency operation requires attention to materials and construction. MLCCs (multilayer ceramic capacitors) offer very low ESR, often in the range of tens of milliohms at 1 MHz, making them ideal for resonant circuits. These capacitors also have excellent high-frequency performance and thermal stability. In this design, a 4.7 nF MLCC was used, providing a balance between performance, availability, and cost.

## 4.2. Filter Components

The design of the input and output filters emphasizes the minimization of size to achieve high power density while ensuring that all components meet the necessary electrical specifications for optimal performance.

### 4.2.1. Filter Inductors

The inductors in the input and output filters were designed to maintain a current ripple of 15%, a trade-off between efficiency, size, and stability. The required inductance was calculated using Equations (12) and (13), derived from the inductor voltage definition (Equation (11)):

$$V_L(t) = L \frac{di_L}{dt} \quad (11)$$

$$L_{in} > \frac{V_g(T_S - t_3)}{\Delta I_{L_{in}}} \quad (12)$$

$$L_{out} > \frac{V_o(t_3 - t_1)}{\Delta I_{L_{out}}} \quad (13)$$

where

$\Delta I_L$ : Current ripple.

Obtaining the following values:

- $L_1 > 32.06 \mu\text{H}$ .
- $L_2 > 33.06 \mu\text{H}$ .
- $L_3 > 33.06 \mu\text{H}$ .

For all the filter inductors, a 47  $\mu\text{H}$  inductor was selected for the experimental design.

#### 4.2.2. Filter Capacitors

The capacitors in output filters were designed to maintain a voltage ripple of 0.5%. The required capacitance was calculated using Equations (14) and (15), using charge balancing to obtain Equation (16):

$$Q = \int i \cdot dt; I = \frac{\Delta Q}{\Delta t} \quad (14)$$

$$Q = C \cdot V; \Delta Q = C \cdot \Delta V \quad (15)$$

$$I_{out} = \frac{C_{out} \cdot \Delta V_{out}}{\Delta t}$$

$$C_{out} > \frac{I_{out}}{\Delta V_{out} \cdot f_S} \quad (16)$$

- $C_{o2} > 15.5 \mu\text{F}$ .
- $C_{o1} > 5 \cdot C_{o2,mini}; C_{o1} > 77.5 \mu\text{F}$ .

For the filter capacitors, standard 100  $\mu\text{F}$  electrolytic capacitors were selected for the experimental design.

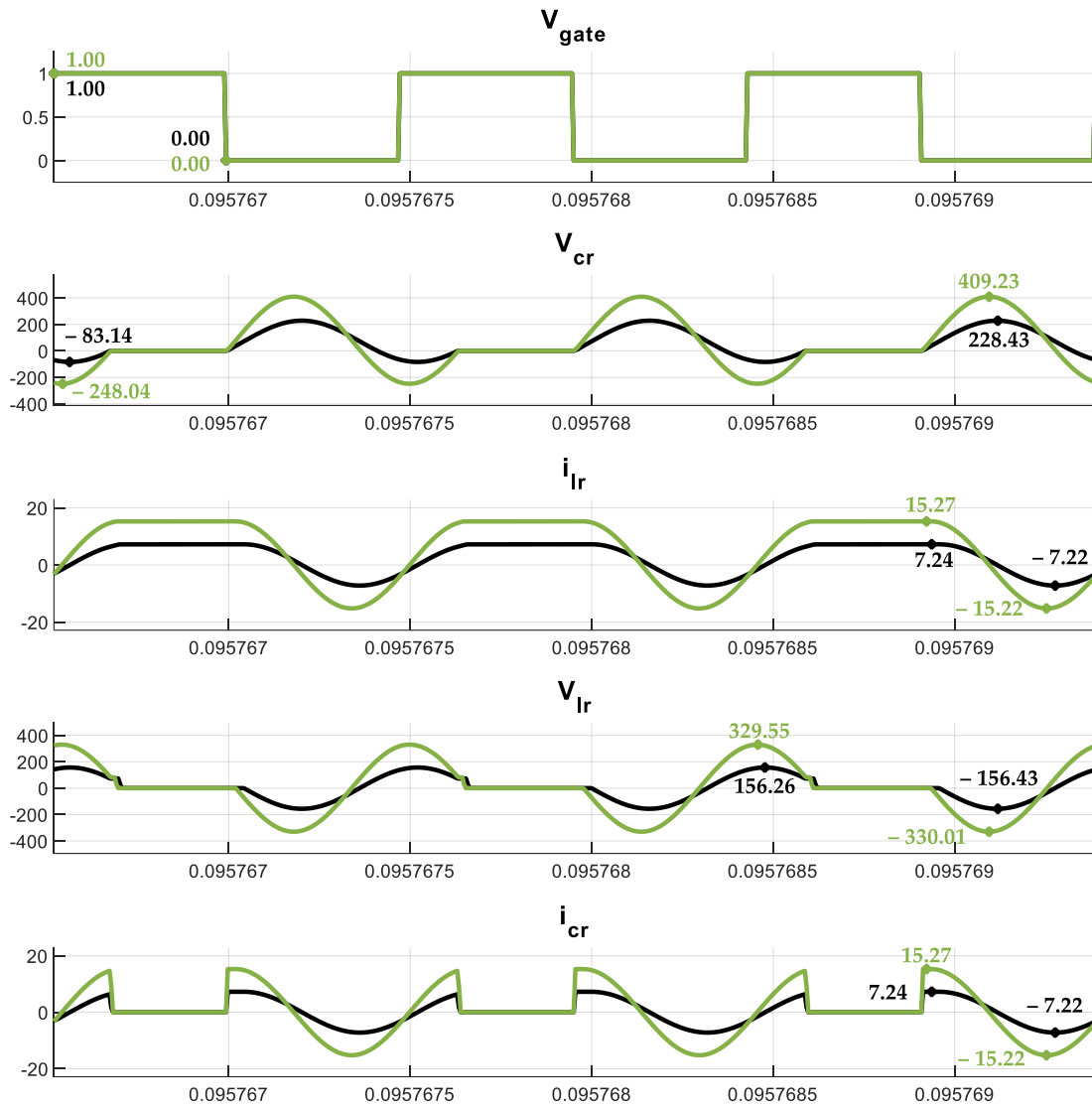
### 5. Simulation Model and Results

In order to verify the ZVS QR Cuk–SEPIC full-wave combined converter analysis; a simulation model has been implemented using Matlab/Simulink R2024b software (Version 24.2 R2024b). The implemented topology is shown in Figure 3. First, the operation in step-down mode was simulated for an input voltage of 48 V, to obtain a symmetrical output voltage of  $\pm 24$  V, with a load variation of  $R_1$  and  $R_2$  between 4.7  $\Omega$  (245.1 W) and 10  $\Omega$  (115.2 W), maintaining the resonant action. For this purpose, the  $L_R$ – $C_R$  resonant tank has been dimensioned to satisfy the zero voltage, full-wave condition:  $(V_g + V_{o1}) < \left(I_g + \frac{V_{o1}}{R_1} + \frac{V_{o2}}{R_2}\right) \cdot Z_o$ .

Secondly, the operation in boost mode was simulated for an input voltage of 12 V, obtaining a symmetrical output voltage of  $\pm 24$  V. In addition, the model was subjected to the same load variations, also between 4.7  $\Omega$  (245.1 W) and 10  $\Omega$  (115.2 W). The simulation results obtained are shown in Figures 9 and 10. These results reproduce and confirm the previous analysis, whose waveforms are shown in Figure 8. The model was simulated with the parameters provided in Table 1, in step-down mode, setting the operating frequency at 1.044 MHz, with a minimum *off-time* of 331 ns and in step-up mode, at a frequency of 521.72 kHz, with a minimum *off-time* of 364 ns. In both cases, to achieve the resonant action,  $t'_2 < t_{off} < t_2$ .

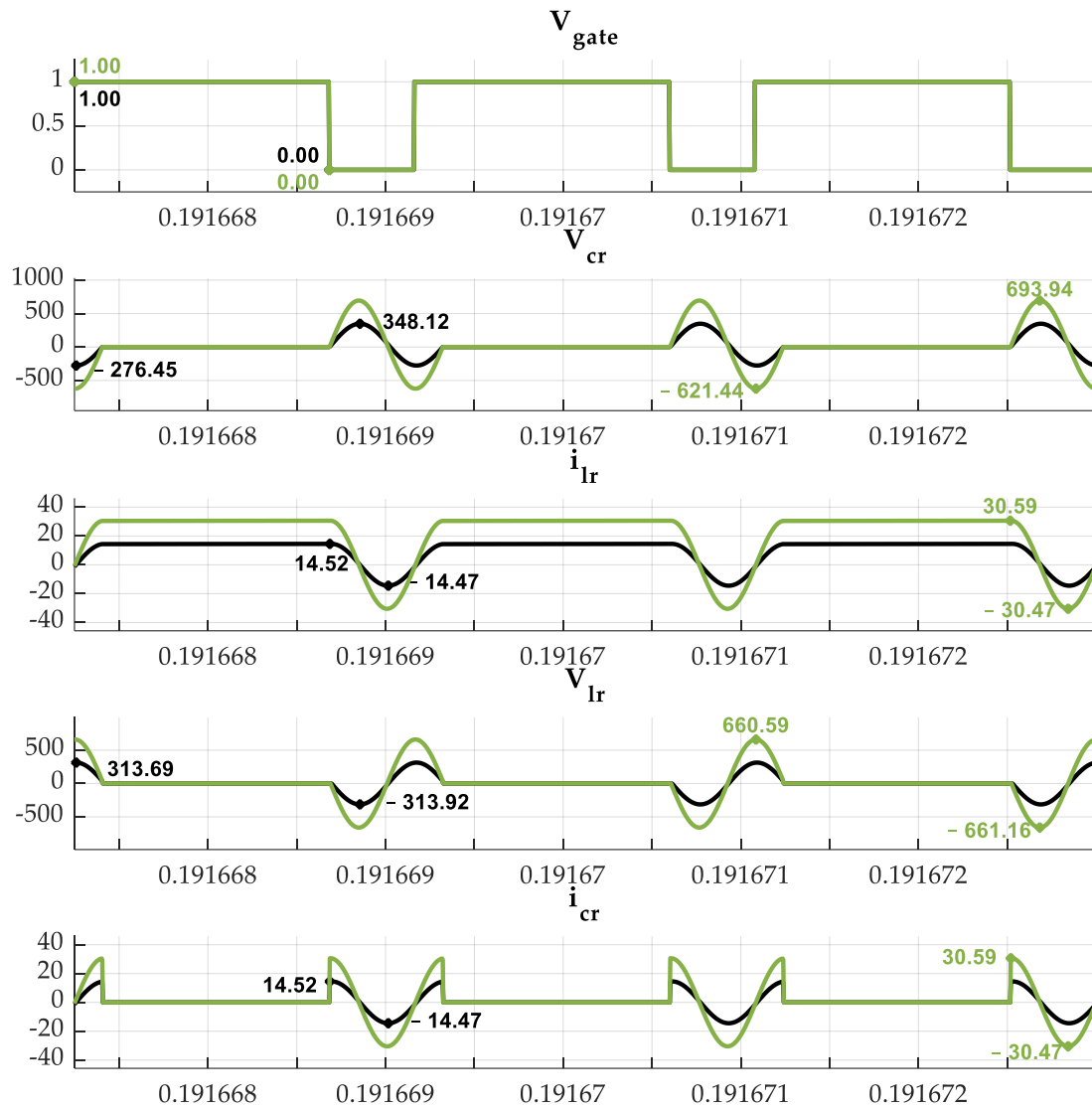
**Table 1.** Parameters of the simulated ZVS QR Cuk–SEPIC full-wave combination converter model.

Parameter	Value
Resonant Inductor ( $L_R$ )	2.2 $\mu\text{H}$
Resonant Capacitor ( $C_R$ )	4.7 nF
Switching Frequency ( $f_s$ )	522 kHz–1.044 MHz
Input Voltage ( $V_g$ )	48–12 V
Output Voltages ( $V_{o+}, V_{o-}$ )	$\pm 24$ V
Load Resistors ( $R_{o1}, R_{o2}$ )	4.7–10 $\Omega$
Power	245.1–115.2 W



**Figure 9.** Simulation results of the ZVS QR Cuk-SEPIC full-wave combination converter in step-down mode ( $V_o/V_g = 24/48$  V), with a load variation between  $4.7 \Omega$  (green line) and  $10 \Omega$  (black line) at 1.044 MHz.

From the theoretical analysis and from the maximum and minimum values showed in Figure 8, the peak voltage in the resonant capacitor at 115 W ( $10 \Omega$ ) can be estimated to reach the maximum value as  $v_{C_{R,Peak}}(max) = V_g + V_{o1} + (I_g + I_{o1} + I_{o2}) \cdot Z_o = 227.77$  V and the minimum value as  $v_{C_{R,Peak}}(min) = V_g + V_{o1} - (I_g + I_{o1} + I_{o2}) \cdot Z_o = -83.77$  V. The simulated maximum and minimum values (Figure 9) are 228.43 V and  $-83.14$  V, respectively, with a 0.3% error (0.66 V). The remaining maximum and minimum simulated values were compared with the theoretical values, shown in Figure 8, providing relative differences of less than 1%.



**Figure 10.** Simulation results of the ZVS QR Cuk-SEPIC full-wave combination converter in step-up mode ( $V_o/V_g = 24/12$  V), with a load variation between  $4.7 \Omega$  (green line) and  $10 \Omega$  (black line) at  $521.72$  kHz.

## 6. Loss Estimation Model of the Combined SIBSO Converter

In order to simulate the operation of the converter in “non-ideal” conditions and estimate its efficiency, parasitic components have been added to the simulation model, such as voltage drop in the diodes, conduction resistance of the GaN FET, series resistors of all inductors and capacitors (ESR) and parallel resistors of the filter inductors (EPR). In the background, we aim to perform a loss analysis and estimation that, by considering the RMS current analysis for each component and the involved non-idealities, allows us to estimate the losses in the components involved in the combined SIBSO converter. A theoretical analysis of this estimation can be found in references [33–35]. The values considered are those provided in the technical datasheets by the manufacturers, for the components summarized in Table 2. A model in Matlab/Simulink has been implemented in order to estimate each component’s losses and the converter efficiency.

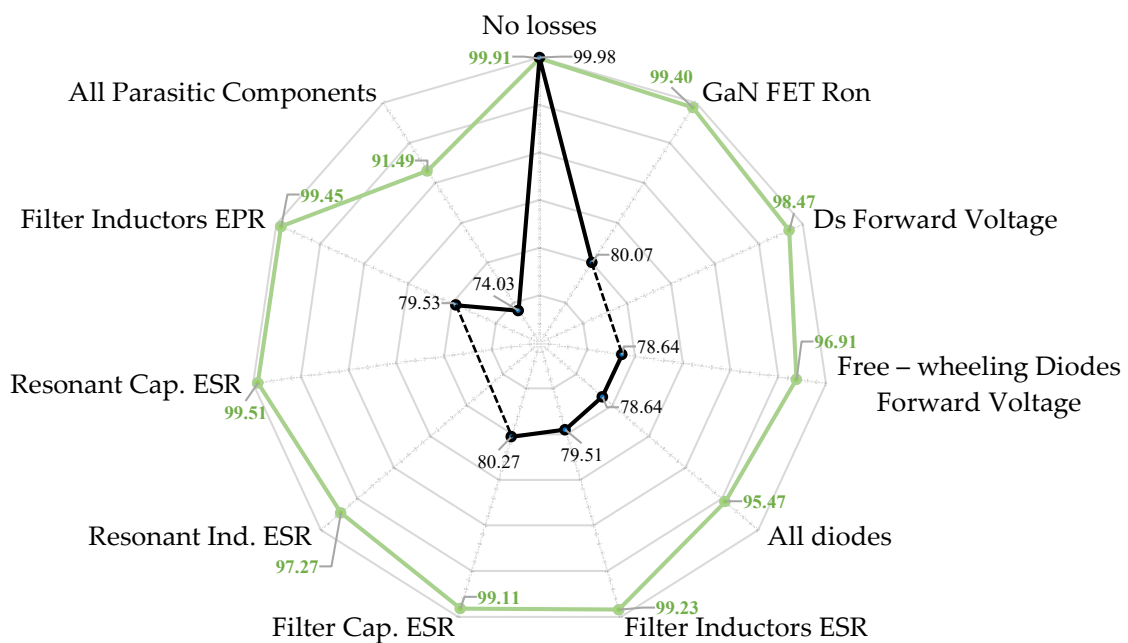
**Table 2.** Values of the non-ideal components for the loss estimation model.

Component	Non-Ideal Value
GaN FET on Resistance	TP65H035G4WSQA 41 mΩ
Diode Forward Voltage	VB30202C 0.7 V
Filter Inductors	47 μH
	55 mΩ (ESR) 1 kΩ (EPR)
Filter Capacitors	100 μF 30 mΩ
Resonant Inductor (Air core)	2.2 μH 120 mΩ
Resonant Capacitor	4.7 nF 30 mΩ

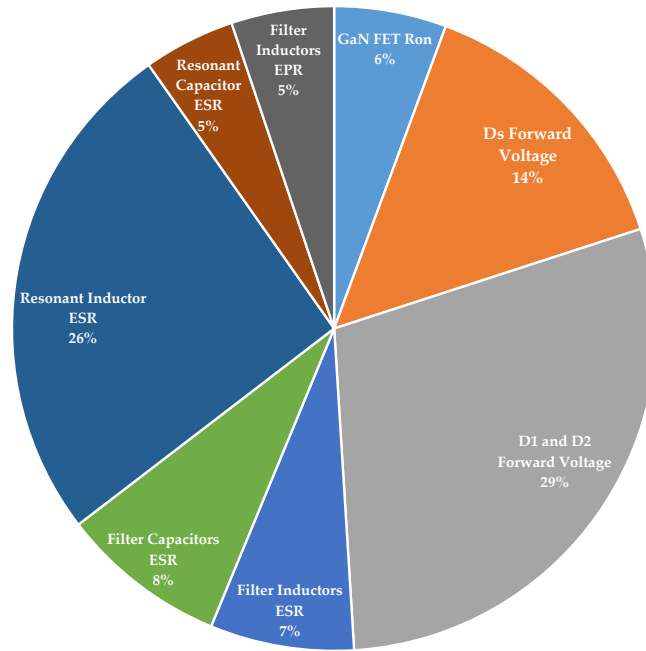
First, the model was simulated with ideal components, obtaining an efficiency reaching 100%. Then, each of the non-idealities of each component considered were added one by one, and finally, all of them were simulated together. In addition, the conventional hard-switching converter (without a resonant tank) has also been simulated using the same parasitic values as in the model with soft-switching.

To take into account the loss due to hard-switching, a snubber network has been added to the main switch, calculating the values for  $R_S$  and  $C_S$  as a function of the parameters  $E_{on}$  (turn on switching energy) and  $E_{off}$  (turn off switching energy) provided by the manufacturer.

These results are shown in Figure 11, where the influence of each component on the efficiency of the converter, individually and overall, is analyzed. Furthermore, the advantage of the proposed converter (green line) is verified, as the losses of the conventional converter (black line) would be much higher due to hard-switching losses at 1 MHz. As a result, to obtain losses similar to the resonant converters, the operating frequency must be lowered to 80 kHz. Figure 12 shows the percentage distribution of losses in each component for the same conditions.

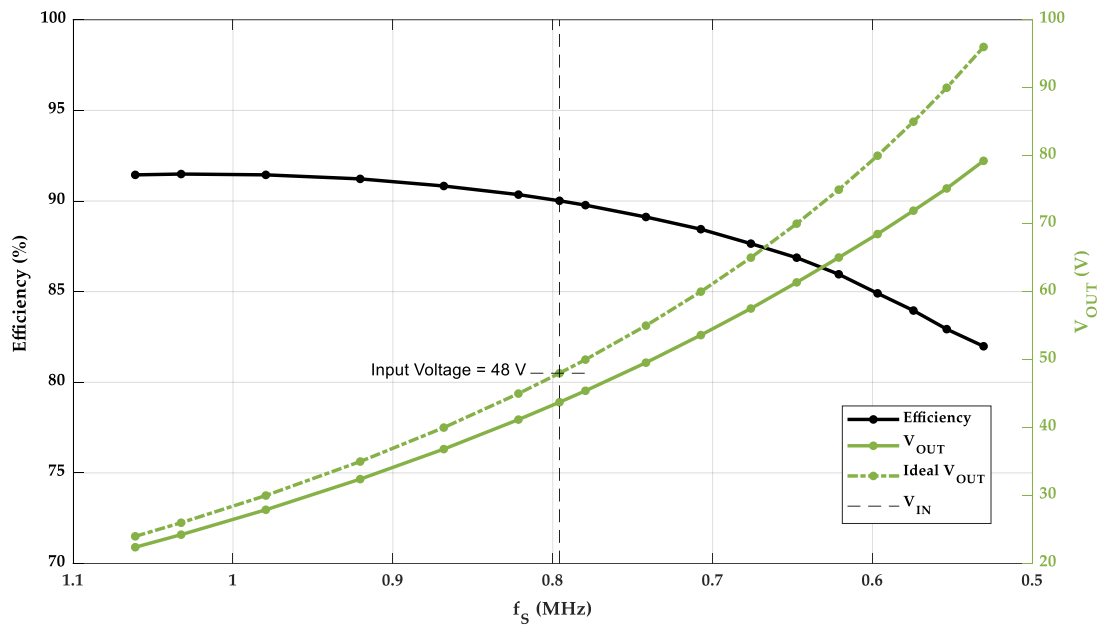


**Figure 11.** Simulated efficiency with non-ideal parameters for each component at 1 MHz. Black line: Non-resonant combination converter. Green line: ZVS QR combination converter.



**Figure 12.** Estimation of percentual power losses in each component for the proposed combination converter.

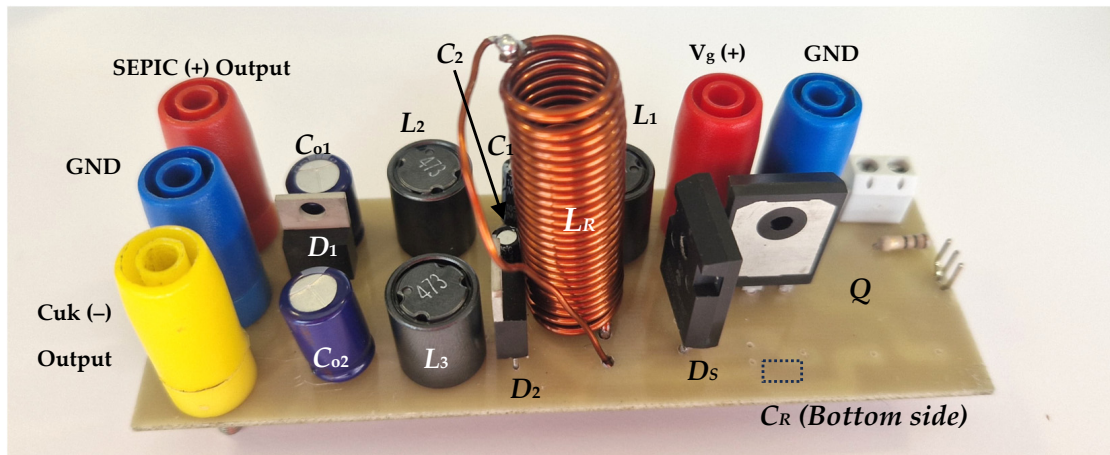
Although the above simulations have been performed for a voltage conversion ratio of 0.5 ( $m = 2/3$ ) mainly to show high-frequency operation, the converter can also operate at other conversion ratios, so in Figure 13, a frequency sweep between 500 kHz and 1 MHz is performed, operating the converter in both step-up and step-down modes and measuring the efficiency and output voltage. The input voltage is set at 48 V, while the output voltage changes between 22 and 80 V (voltage conversion ratio of 1.5,  $m = 2/5$ ) and the efficiency varies between 92 and 82%.



**Figure 13.** Simulated efficiency and output voltage of the proposed configuration for different conversion ratios.

## 7. Experimental Results

In order to verify the previous analysis and simulation results, an experimental prototype based on the configuration proposed in this work has been implemented, which is shown in Figure 14. The most relevant waveforms have been measured, mainly those related to resonant operation, also verifying that soft-switching at zero voltage occurred.



**Figure 14.** Experimental prototype of the ZVS QR Cuk–SEPIC full-wave combination converter.

The prototype was tested in an open-loop configuration, using the UCC5304DWV driver specifically engineered for GaN FETs. In addition, a GaN FET was employed as the main switching element, enhancing low-loss and high-frequency performance. This open-loop setup enabled an isolated evaluation of the converter response and allowed for a detailed analysis of the more relevant resonant waveforms. The integration of the UCC5304DWV driver with a GaN FET enabled precise control over the switching operation, ensuring optimal performance and minimizing losses before the implementation of closed-loop control strategies. The gate signal was generated digitally by using an ESP32 microcontroller.

### 7.1. Operational Parameters of the Proposed Converter

The prototype operates using a specific set of components and is designed to work within predefined parameters to ensure optimal operation. Key components include capacitors and inductors precise values, especially for the resonant tank, customized to the circuit's requirements, as well as gate driver and semiconductor devices. The prototype is designed to operate with a voltage conversion ratio of  $V_o/V_g = 24/48$  V for an output power of 144 W (72 W in each output). A summary of the components used and the parameters of the converter is provided in Table 3. This table shows specifications, including the selected semiconductor devices, passive components, and most relevant parameters.

**Table 3.** Operational parameters and component values of the experimental setup.

Parameter/Component	Value	Designation
$C_R$	4.7 nF	Resonant capacitor
$L_R$	2.2 $\mu$ H	Resonant inductor
$f_s$	1043.81 kHz	Switching frequency
$f_o$	1565.16 kHz	Resonant frequency
$t_{off}$	396–638 nS	Required <i>off</i> -time

Table 3. Cont.

Parameter/Component	Value	Designation
$V_o$	24 V	Output voltage
$V_g$	48 V	Input voltage
$Z_o$	21.6 $\Omega$	Characteristic impedance
TP65H035G4WSQA	$R_{ON} = 41 \text{ m}\Omega$	GaN FET
VB30202C	$V_f = 0.7 \text{ V}$	Diodes
$R_{o1}, R_{o2}$	8 $\Omega$	Load resistors
$C_{o1}, C_{o2}$	100 $\mu\text{F}$	Output capacitors
$L_1, L_2, L_3$	47 $\mu\text{H}$	Filter inductors

### 7.2. Gate Drive Circuit Overview

The UCC5304 is an isolated gate driver designed to control power transistors like MOSFETs or GaN FETs, ensuring safe operation through a galvanic isolation barrier. The driver receives a control signal at the IN pin, processed by the under voltage detector UVLO and input logic block, which ensures proper operation only when the input voltage is within the required range. The processed signal crosses the isolation barrier and is received by the level shift and control logic, which drives the totem pole output stage. This output stage provides the necessary gate drive current at the OUT pin to switch the external power transistor efficiently. The UCC5304 is particularly suited for GaN FETs in high-frequency applications, where fast switching is essential for performance and efficiency. A diagram block of this driver is shown in Figure 15. All the data related to the driver are available in [36]

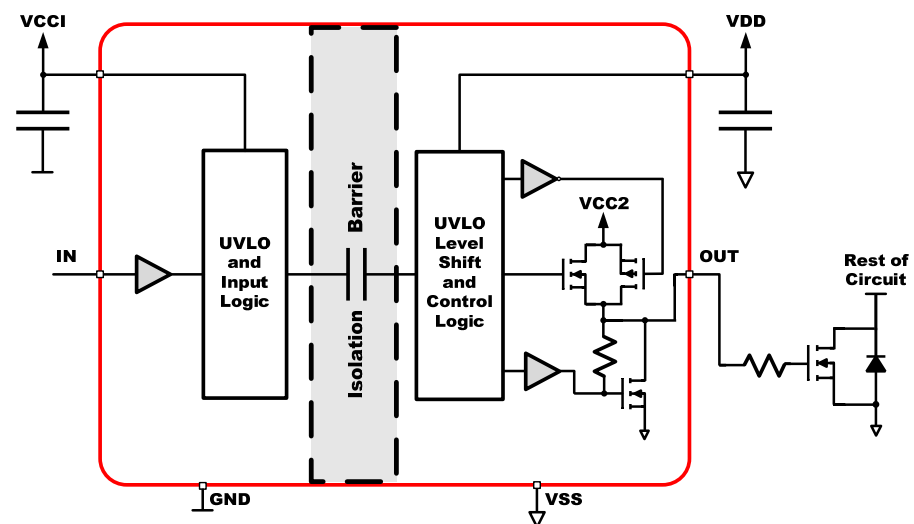
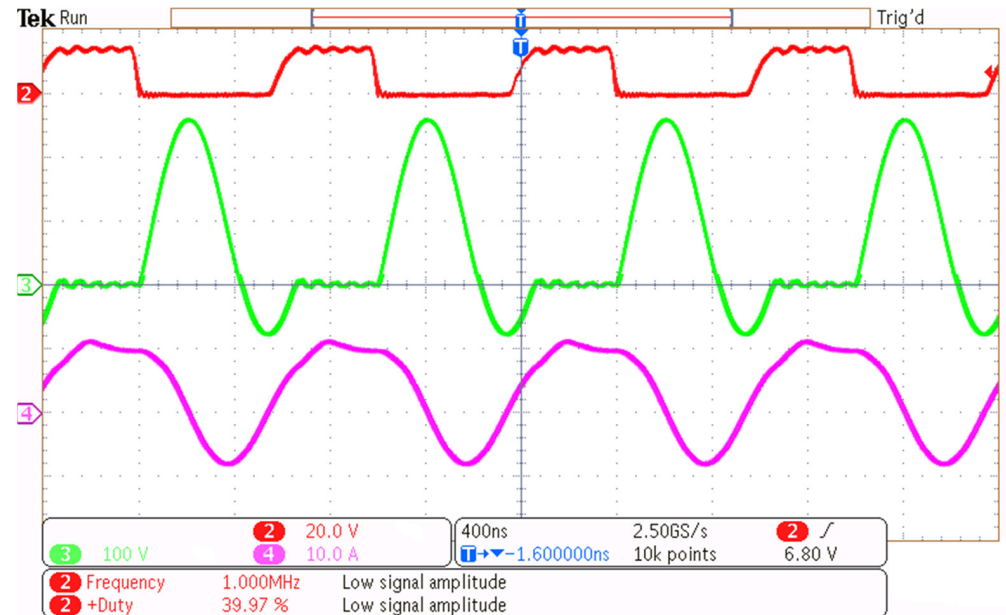


Figure 15. Block diagram of the UCC5304 isolated gate driver.

### 7.3. Main Waveforms of the ZVS QR Cuk–SEPIC Full-Wave Combination Converter

The main resonant waveforms,  $V_{C_R}$  and  $i_{L_R}$ , are shown in Figure 16 as well as the main switch excitation signal  $V_{gate}$ . These experimental waveforms of the quasi-resonant converter operating under zero-voltage switching (ZVS) conditions confirm the expected resonant behavior. When the switching device turns off, the energy stored in the resonant inductor transfers to the resonant capacitor, causing the capacitor voltage to rise in a nearly sinusoidal form. This oscillation continues as the voltage develops a full positive half-cycle, ensuring that sufficient time is allowed for the resonant action to occur (Figure 8). The GaN

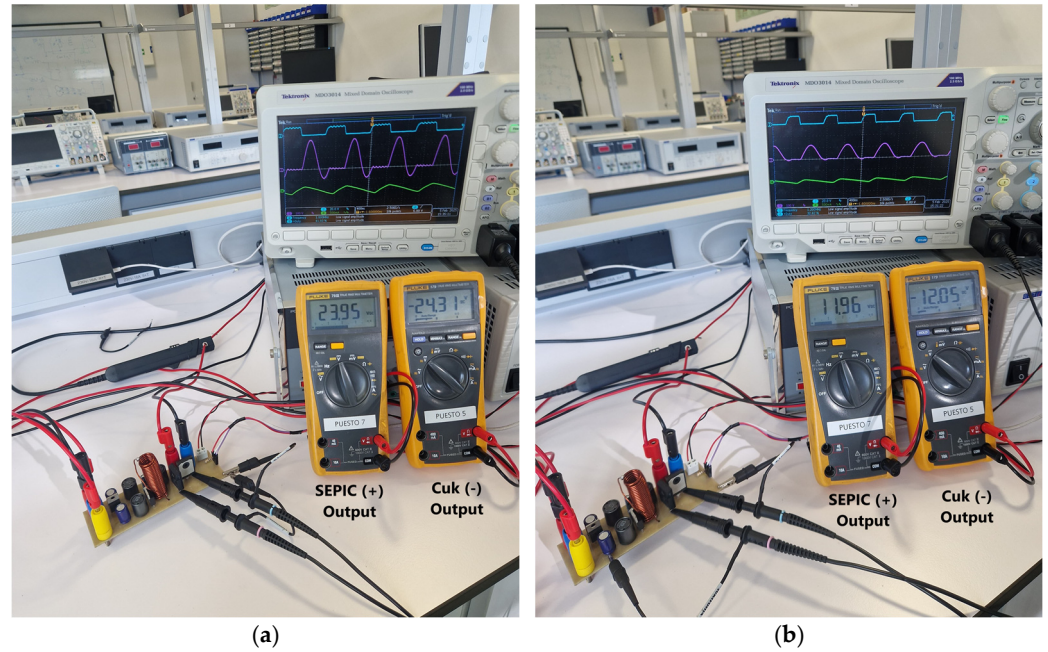
switch must turn on at any point during the negative half-cycle of the resonant capacitor voltage and before this half-cycle ends, allowing the inductor to fully charge. The cycle repeats when the switch turn off again. It can be seen that the maximum value of the voltage at the resonant capacitor reaches the value of 260 V, which theoretically should be 266.72 V.



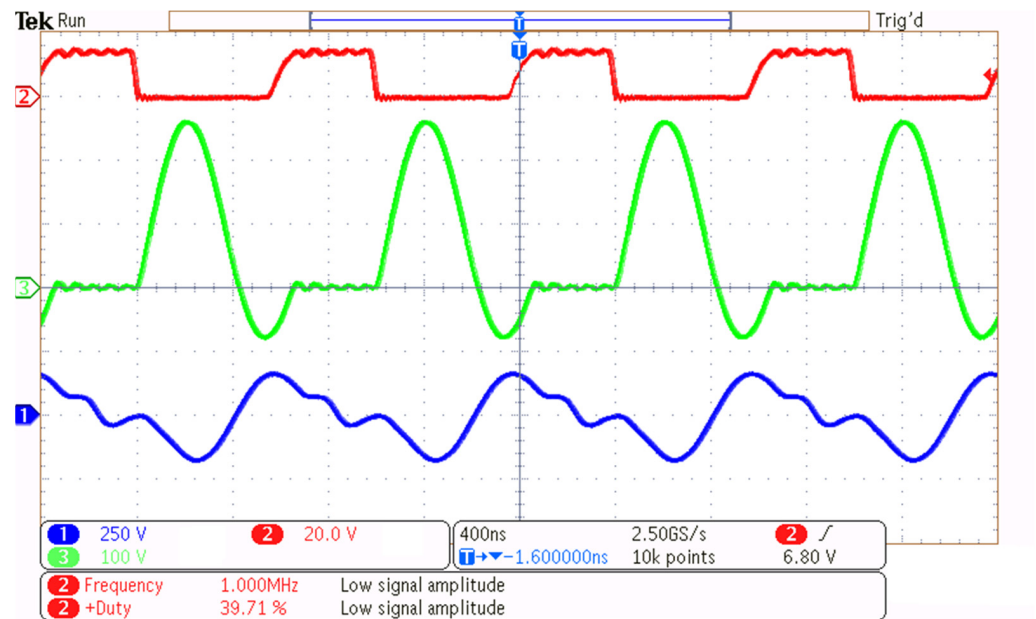
**Figure 16.** Experimental results of the ZVS QR Cuk–SEPIC full-wave combination converter in step-down mode, operating at 144 W. CH 2: Gate signal. CH 3: Voltage in resonant capacitor. CH 4: Current across the resonant inductor.

Figure 17 contains two pictures displaying the experimental results of the prototype converter. In both, the setup includes the converter, an oscilloscope measuring the resonant capacitor voltage along with the input current, and two multimeters measuring the output voltages. In Figure 17a, the converter is operating at a frequency of 1 MHz to provide a bipolar output voltage of  $\pm 24$  V, while in Figure 17b, it is set at 1.26 MHz to deliver  $\pm 12$  V. It can be seen how the second case has nearly no negative half-cycle, as it is at conditions close to the resonance limit.

In the experimental results shown in Figure 18, a small parasitic high-frequency oscillation in the inductor voltage waveform is observed during the interval where it is theoretically expected to remain at zero. This deviation from the ideal response is due to parasitic elements in the circuit, such as parasitic capacitances in the diodes. Despite these imperfections, the overall waveform confirms that the expected resonant action develops. The maximum inductor voltage amplitude varies with operating frequency and load conditions, demonstrating the characteristic behavior of quasi-resonant operation, where higher switching frequencies result in shorter resonant periods and faster voltage transitions. The resonant inductor voltage follows a behavior complementary to the voltage on the resonant capacitor, with polarity inverts corresponding to the oscillatory charging and discharging of the capacitor.

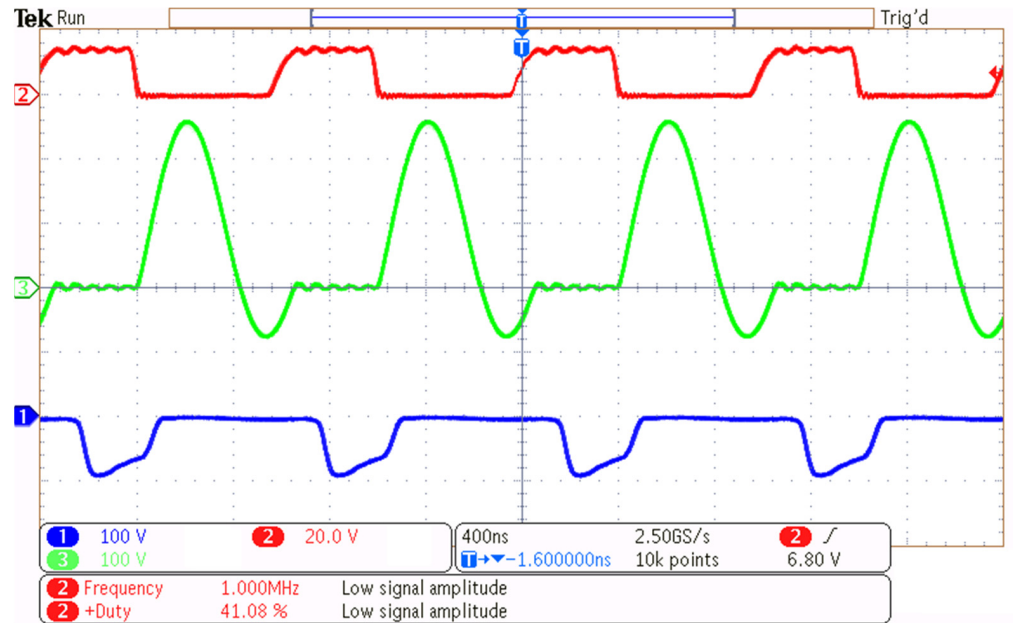


**Figure 17.** Experimental operating set-up of the ZVS QR Cuk-SEPIC full-wave combination converter in step-down mode, operating at 144 W. (a) Converter operating with a conversion ratio of  $V_o/V_g = 24/48$  V. (b) Converter operating with a conversion ratio of  $V_o/V_g = 12/48$  V. In both pictures, left multimeter measures SEPIC output (+) while the right multimeter measures Cuk output (-).



**Figure 18.** Experimental results of the ZVS QR Cuk-SEPIC full-wave combination converter in step-down mode, operating at 144 W. CH 2: Gate signal. CH 3: Voltage in resonant capacitor. CH 1: Voltage in resonant inductor.

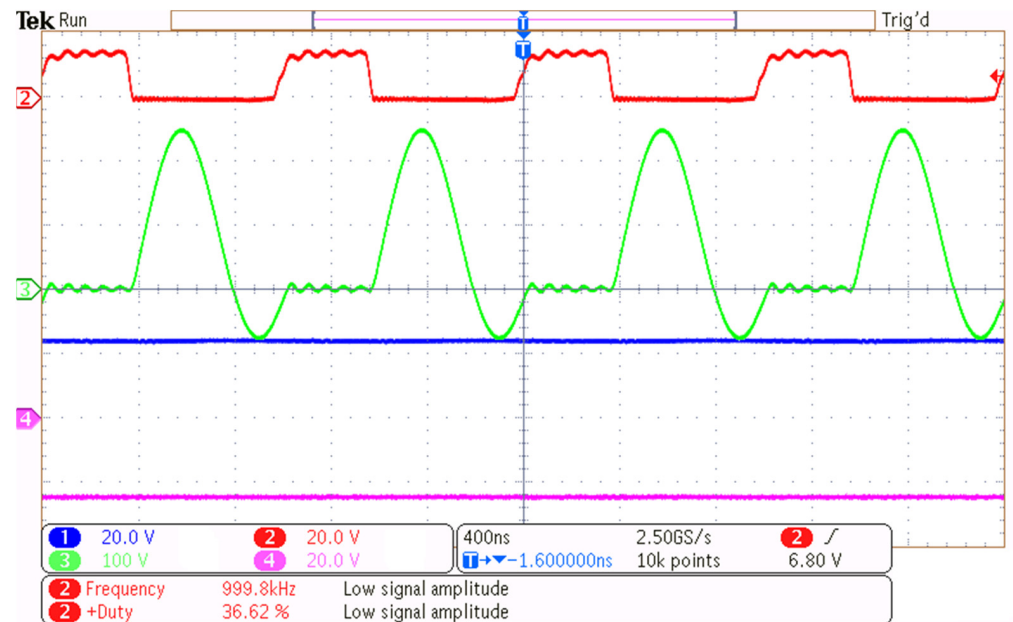
The voltage in the diodes shows some deviation in comparison to the ideal waveform, as the negative value should remain constant. This deviation, which can be observed in Figure 19, is due to the parasitic capacitance of the diodes, although the resulting waveform is similar to the expected behavior and does not affect their function.



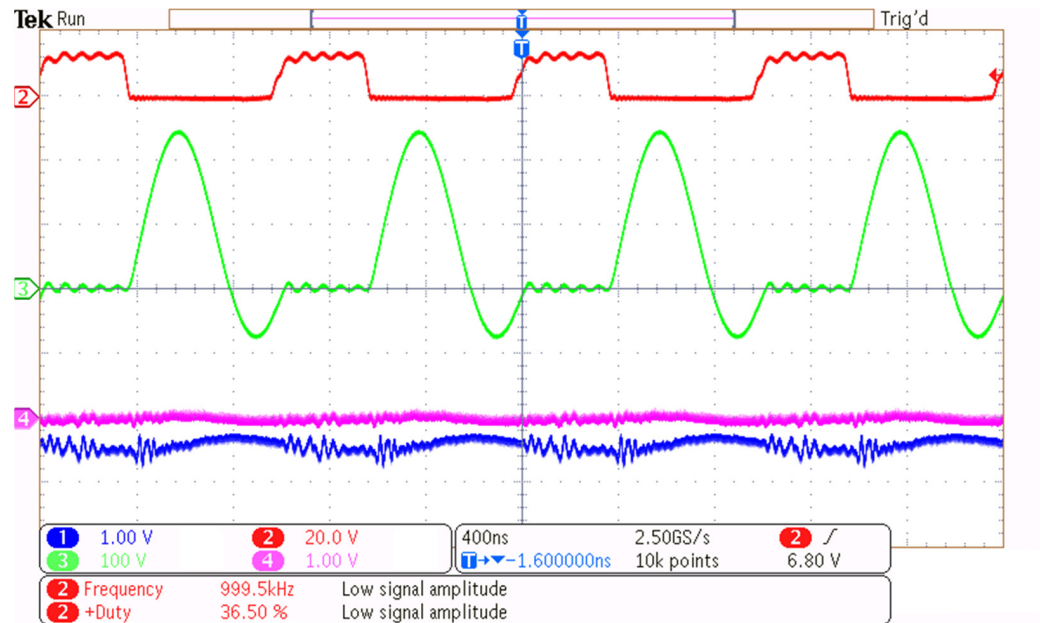
**Figure 19.** Experimental results of the ZVS QR Cuk–SEPIC full-wave combination converter in step-down mode, operating at 144 W. CH 2 waveform: Gate signal. CH 3: Voltage in resonant capacitor. CH 1: Voltage in free-wheeling diode (Cuk).

7.4. Ripple Characteristics

Figure 20 displays the bipolar output voltages, illustrating the symmetrical behavior of the converter. The waveform confirms that the converter generates balanced positive and negative output voltages, maintaining the expected voltage levels. The measured output voltage ripple is also presented in Figure 21.

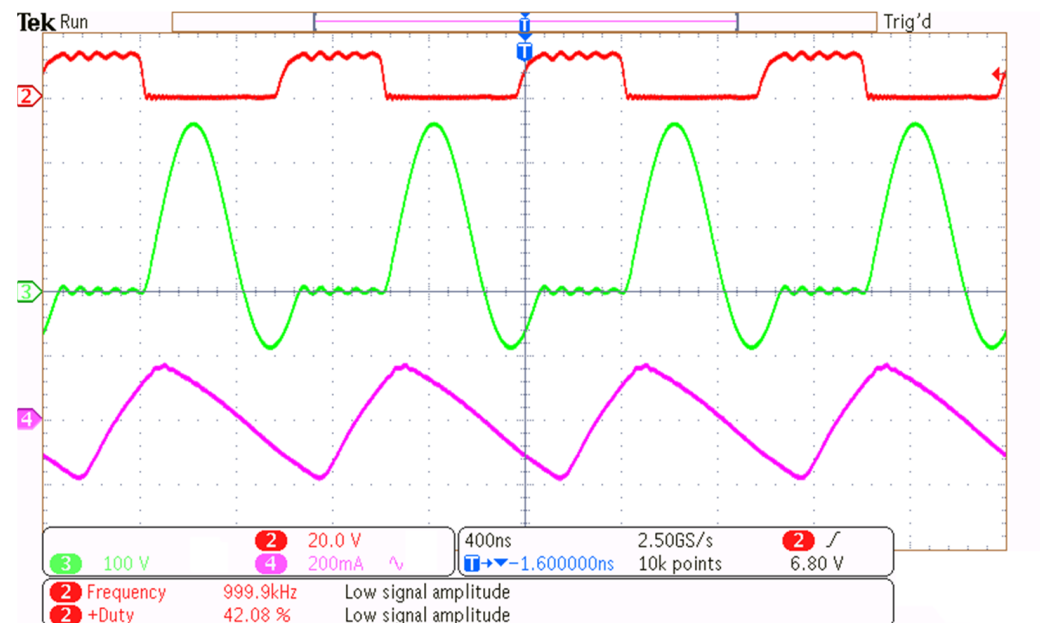


**Figure 20.** Bipolar output voltages of the ZVS QR Cuk–SEPIC full-wave combination converter in step-down mode, operating at 144 W. CH 1: SEPIC (+) output. CH 4: Cuk (–) output.



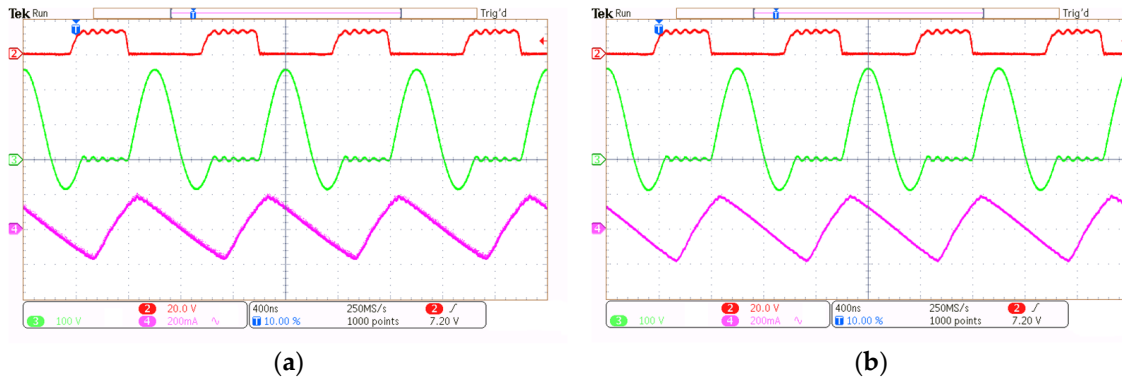
**Figure 21.** Ripple of the bipolar output voltages of the ZVS QR Cuk–SEPIC full-wave combination converter in step-down mode, operating at 144 W. CH 1: SEPIC voltage ripple. CH 4: Cuk voltage ripple.

Meanwhile, Figure 22 shows the input current ripple, which reflects the switching behavior and the effectiveness of the input filtering stage. Controlling the input current ripple is crucial for minimizing electromagnetic interference (EMI). Furthermore, the waveform in Figure 22 confirms that the inductor core operates below saturation, developing the expected waveform.



**Figure 22.** Ripple of the input current (CH 4) of the ZVS QR Cuk–SEPIC full-wave combination converter in step-down mode, operating at 144 W.

Figure 23 shows the output inductor’s current ripple of the ZVS QR Cuk–SEPIC full-wave combination converter. Trace (a) corresponds to the SEPIC output current, while (b) represents the Cuk output current, highlighting its respective ripple characteristics.

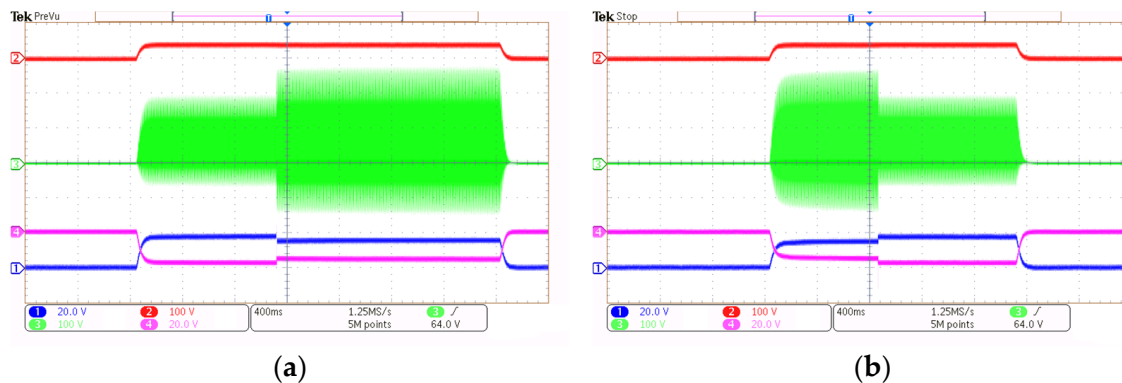


**Figure 23.** Ripple of the output inductor current (CH 4) of the ZVS QR Cuk–SEPIC full-wave combination converter. (a) SEPIC output inductor current. (b) Cuk output inductor current.

### 7.5. Dynamic Response and Stability

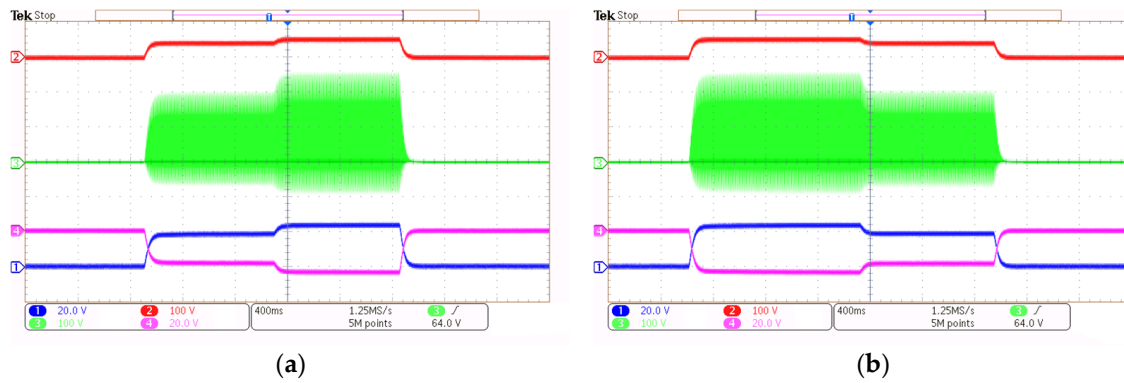
To analyze the dynamic response of the converter, the prototype was subjected to variations in both load and input voltage. These tests were designed to assess the converter’s behavior under different operating conditions, providing valuable insights into its transient performance. Key parameters, such as output voltage and resonant capacitor voltage, were measured to evaluate the system’s response to these variations.

Figure 24 illustrates the dynamic response of the converter when subjected to a 50% load variation. The experiment follows a sequential process: first, the converter is powered on; then, the load variation is introduced; and finally, the converter is turned off. As shown in the figure, the SEPIC and Cuk output voltages (CH 1 and CH 4) exhibit transient behavior in response to the load change, while the resonant capacitor voltage (CH 3) adapts accordingly. The two scenarios presented correspond to an increasing load from 10  $\Omega$  to 5  $\Omega$  (a) and a decreasing load (b) from 5  $\Omega$  to 10  $\Omega$ .



**Figure 24.** Output voltage and resonant capacitor voltage response with a load variation of 50%. CH 1: SEPIC output voltage. CH 2: Input voltage. CH 3: Voltage in the resonant capacitor. CH 4: Cuk output voltage. (a) Load increase. (b) Load decrease.

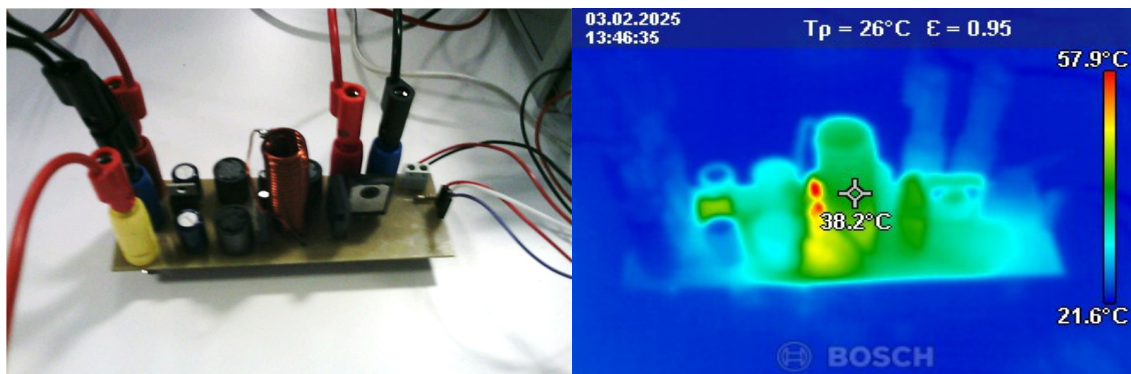
Figure 25 presents the response of the converter when subjected to a 20% variation in input voltage. The procedure consists of powering on the converter, applying the input voltage change, and subsequently turning it off. The SEPIC and Cuk output voltages (CH 1 and CH 4) adjust to the variation, while the resonant capacitor voltage (CH 3) reflects the transient effects. The figure displays two cases: (a) increasing input voltage from 38 to 48 V and (b) decreasing input voltage from 48 to 38 V.



**Figure 25.** Output voltage and resonant capacitor voltage response with input voltage variation of 20%. CH 1: SEPIC output voltage. CH 2: Input voltage. CH 3: Voltage in the resonant capacitor. CH 4: Cuk output voltage. (a) Input voltage increases. (b) Input voltage decreases.

### 7.6. Thermal Response

To understand the thermal distribution of the converter, a thermal camera was used to capture and analyze the temperature variations in all components of the converter. This made it possible to identify possible overheated regions and to evaluate the thermal response. The thermographic images of the experimental prototype under operation shown in Figure 26 reveal that the components experiencing the highest temperature rise are the diodes and the resonant inductors. No heat sinks have been used in the prototype.

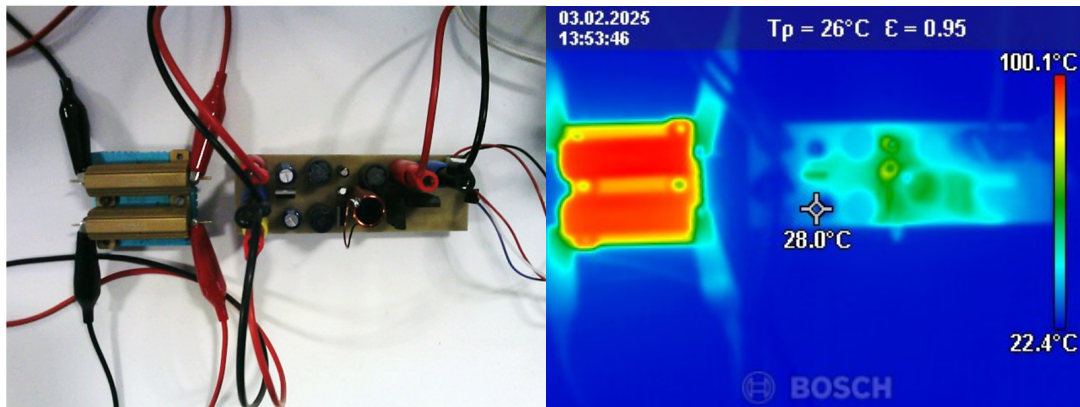


**Figure 26.** Thermal response of the ZVS QR Cuk-SEPIC full-wave combination converter under operation.

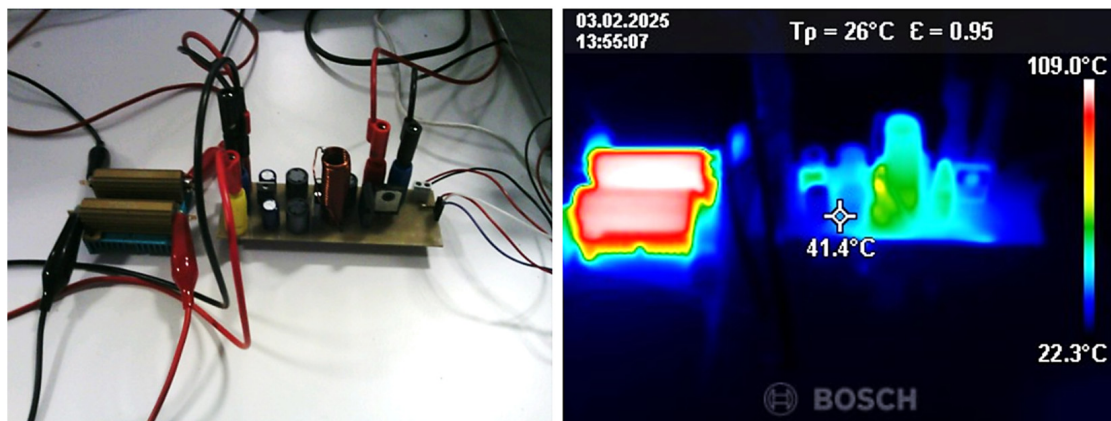
Diodes exhibit significant heating due to their switching and conduction losses, which are inherent to the quasi-resonant operation of the converter. The resonant inductor also shows considerable temperature rise due to the high RMS currents flowing through it. These currents increase conduction losses, which are increased by the inductor's equivalent series resistance (ESR). The ESR results from the use of an air-core inductor, which is necessary to minimize core losses at high switching frequencies. In contrast, the gallium nitride (GaN) device remains notably cooler than the other components, attributed to the implementation of soft-switching, which minimizes switching losses and reduces the total power dissipation. The combination of GaN FET technology and quasi-resonant operation enhances the converter's efficiency, as lower energy is lost as heat, leading to improved thermal response.

Figures 27 and 28 show the converter placed next to the load resistors. This setup allows for a direct comparison of the temperature distribution between the converter and the resistive loads. The image clearly illustrates the thermal gradient, with the load resistors reaching much higher temperatures due to their function as power-dissipating elements.

This contrast highlights the power distribution of the converter, as its core components maintain relatively lower temperatures, further supporting the benefits of GaN-based designs in reducing thermal management.



**Figure 27.** Thermal response of the ZVS QR Cuk-SEPIC full-wave combination converter under operation. Top view.



**Figure 28.** Thermal response of the ZVS QR Cuk-SEPIC full-wave combination converter under operation. Front view.

### 7.7. SIBSO DC-DC Converter Efficiency

The method to estimate the efficiency has been the measurement of the average values of the voltage  $V_g$  and current across the inductor  $L_1$ . With the product of these values, the input power was obtained. To calculate the output power, the output voltage was measured at each of the outputs, as well as the current through each of the loads. The voltage-current product was calculated for each output and then the sum of the two was added together to obtain the output power. Finally, the average measured efficiency, calculated as the ratio between output and input power, was 89.2%. For the voltage and current measurements, Fluke 179 multimeters were used, taking ten samples for each measurement and then considering the average.

The experimental prototype shows similar results to the simulated one, with differences due to the non-idealities of the components, such as parasitic capacitances and inductances, which slightly modify the expected waveforms. However, the results obtained show a good approximation to the waveforms of the simulated model with parasitic components, as well as in the maximum/minimum values. It should be taken into account that is not exactly the same, since the simulation model has taken into account the most relevant parasitic components, but not consider, for example, the parasitic capacitances associated

with the diodes, which causes the deviation that can be seen in Figures 18 and 19. Although this value can be approximated, it is a dynamic value that depends on the operating point of the component, so it is not easy to obtain an exact value. However, this does not significantly affect the converter operation, so it is assumed in order to compare the difference with the theoretical result, which, as can be seen in Figure 8, presents a minimal difference. This section concludes with a comparative table of other multiple-output topologies, which is attached in Table 4.

**Table 4.** Comparison with other references.

Reference	[34]	[35]	[37]	[38]	[39]	SIBSO DC-DC GaN FET
Conversion ratio	24 ÷ 48/±40 V	20 ÷ 50/±15 V	96/±200 V	180/32 V	27/±24 V	48/±24 V
$f_s$	100 kHz	1 MHz	30 kHz	1 MHz	30 kHz	1 MHz
Power	600 W	60 W	450 W	500 W	200 W	150 W
Voltage Stress	$\frac{V_{in} \cdot D}{1-D}$	$V_{in}$	$\frac{V_{in} \cdot D}{1-D}$	-----	$\frac{V_{in}}{1-D}$	$V_{in} + V_{o1} + Z_o \cdot (I_g \cdot I_o)$
Switches	1	2	1	2	4	1
Diodes	2	2	2	2	0	3
Capacitors	5	4	4	3	3	4
Inductors	4	2	4	3	3	3
Floating Driver	No	No	No	Yes	Yes	No
Voltage Gain	$\pm \frac{D}{1-D}$	$\pm D$	$\pm \frac{D}{1-D}$	$\pm \frac{D}{1-D}$	$\pm \frac{D_1}{1-D_1}$	$\pm \frac{1-m}{m}$
Resonant Converter	No	Yes	No	Yes	No	Yes
Power Density	-----	150 W/in <sup>3</sup>	10.5 W/in <sup>3</sup>	-----	7.4 W/in <sup>3</sup>	44.3 W/in <sup>3</sup>
$\eta$	87%	94.6%	85.3%	84.3%	92%	89.2%

The proposed SIBSO DC-DC GaN FET converter offers a balance between efficiency, component count, and power density when compared to other state-of-the-art designs. With a power density of 44.3 W/in<sup>3</sup>, it ranks second among the listed references, notably below [35], which reports 150 W/in<sup>3</sup>, but higher than others such as [37] (10.5 W/in<sup>3</sup>) and [39] (7.4 W/in<sup>3</sup>). It operates at 1 MHz, matching [35,38], which supports compact passive components and improved transient response. In terms of components, this design uses a single, ground-referenced switch, which is the same as [34,37], and better than [35,37,38], indicating a simpler control stage. However, the SIBSO proposed topology requires three diodes, slightly more than most references that use just two [34,35,37,38]. With respect to filter components, it uses four capacitors and three inductors, which is on par with or only slightly above several other implementations.

Regarding efficiency, this SIBSO converter reaches 89.2%, placing it above [34,37], and [38], but below [35] (94.6%) and [39] (92%). Overall, while the proposed SIBSO design does not exceed all references in every metric, it presents a well-rounded solution with high switching frequency, good efficiency, and good power density, supported by a relatively simple switching structure—making it suitable for compact, medium-power applications where soft-switching and integration are priorities.

In terms of costs, the proposed converter offers a cost-effective design by using a single, ground-referenced switch, which reduces the need for complex gate drivers and simplifies control. Additionally, its high switching frequency (1 MHz) enables the use of smaller, lower-value passive components, potentially reducing overall cost compared to lower-frequency designs like [34,37]. Regarding power density (44.3 W/in<sup>3</sup>), while significantly higher than [37] (10.5 W/in<sup>3</sup>) and [39] (7.4 W/in<sup>3</sup>), it remains below [35] (150 W/in<sup>3</sup>).

## 8. Conclusions

This paper proposed a new ZVS QR Cuk–SEPIC full-wave combination converter with bipolar output (SIBSO). An analysis of the operating principle of the converter was presented, followed by detailed simulations to show its operation principles under various conditions. A simulation model was also implemented for efficiency estimation, which provides valid data on the behavior and efficiency of the converter. Besides some drawbacks, like the ability to provide electrical isolation and increased voltage and current stress on the switching devices and passive components due to the addition of the resonant tank, which impairs the topology in high-voltage applications, the full-wave quasi-resonant SEPIC-Cuk topology simulation model results were fitted to experimental results, validating its accuracy and providing a tool for further optimizations. The converter operated at a switching frequency of 1 MHz, achieving an output power of around 150 W with an efficiency close to 90%. These results demonstrate the potential of the SIBSO converter for low-voltage bipolar applications, where both efficiency and compactness are critical. Experimental validation was carried out in an open loop, confirming the theoretical predictions, and showing a good alignment between simulation and experimental results. Additionally, thermal response tests showed that the converter operates without significant temperature rise under typical conditions, indicating effective thermal management. The proposed topology shows interesting power densities and efficiencies combining traditional Cuk and SEPIC topologies with only a resonant tank in the power switch to ensure ZVS full-wave at around 1 MHz. This work provides a transformerless, symmetric bipolar output solution capable of operating in both step-down and step-up modes with a limited number of components. Regarding the proposed closed-loop control, the resonant tank hardens the design of the control strategy, as the modulator must be operated at a constant turn-off time. The next work is to design suitable modulators and feedback controllers, together with testing the stability and transient behavior of the obtained solutions when using variable electronic loads with input inductive capacitive filtering.

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**Data Availability Statement:** This study presents the main data needed by engineers to reproduce the simulations and experiments. Non-essential data used in this study is available on request from the corresponding author. This data is not publicly available as it is well known by experts in the field, and common variations on non-essential data do not change the results.

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