

Can any of the most used phase locked loop circuits be considered as the universal?

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Abstract—This paper aims to highlight the drawbacks of the most common phase locked loop (PLL) circuits to operate as universal PLLs. The phase locked loop tracks the phase of an input signal. These devices are necessary in different disciplines for which the input signal conditions are very different. In fact, they are used in synchronization to the grid waveforms, in the communications applications as frequency modulation or amplitude modulation, and in the measurement of the motors speed, among others. For each discipline, a different group of PLLs is used. Among all of them, the most appropriate to be used in several disciplines seems to be the designed to synchronize the grid. So, they are the chosen to be studied and test their behavior in different applications to find out the PLL which is useful in any application and which achieves to track the phase/frequency signal whose value is initially unknown. I. e. the universal PLL, useful in all the considered applications.

Keywords—phase locked loop, frequency locked loop, modulated frequency, distortion

I. INTRODUCTION

Phase locked loop was initially designed to track the phase of an input periodic signal. It involves different applications: communication systems, microprocessors, dc motor drives, [1], or mechanical encoders, [2]. In recent decades, with the promotion of renewable installations to generate electricity and, in general, the distributed generation, a new application for the PLL appears: the synchronization of dc/ac converters to the grid, [3]-[6]. This new application introduces the necessity of constructing the input signal, eliminating its distortion, i.e. generating the fundamental component corresponding to the input signal. This PLLs capacity makes them an essential tool in other disciplines as the electric power quality, [7]-[8] or the electrical measurement, [9], among others.

However, the work conditions in those different applications are not similar. In the synchronization to the grid, the frequency is 50/60 Hz and it suffers very little modifications. On the contrary, due to the proliferation of the non-linear loads in the power systems, the signal to be tracked in the synchronization uses to be distorted. In the communications, the main procedures are frequency modulation and amplitude modulation. Their frequency ranges are 87.5-108 MHz and 530-1710 kHz, respectively. As can be seen, now, the frequency shifts in a wide range (above all, compared to the fix value of the synchronization).

In addition, the signal to track usually presents little, if not zero, distortion.

In communications, a modulation algorithm is used to modulate the input signal and another algorithm (demodulation) is used to reconstruct it. The demodulation algorithm, which plays the role of the PLL, works with the frequency as a known parameter. This restriction could change if there was a PLL which works in wide ranges of frequencies, able to perform frequency sweeps.

Finally, in the case of dc motor drives or mechanical encoders, the ranges of frequencies are very wide and quickly changing. To do this measurement, the most usual device is the encoder. The procedure followed by this equipment can be translated to a computational algorithm as a zero-crossing detector, which can not be used if the input signal presents noise, even if its level is low.

Thus, the behaviour of the most used PLL to synchronize the grid, are assessed in this paper, to check their operation in the conditions imposed by applications different from those for which they were designed. Those applications chosen are framed in electrical and electronics disciplines, for simplicity.

The paper is organized as follows: in section II the most used PLLs for synchronization are presented. In section III the results provided by those PLLs are presented, when they are applied to a distorted 50 Hz signal. In section IV, those PLLs are applied to an input signal corresponding to a different application and the results are presented and analysed. Finally, some conclusions are drawn in section V.

II. THE MOST USED PLLS IN SYNCHRONIZATION

As indicated above, in communications, the demodulation algorithm works with an input signal whose frequency value is known. For this reason, the PLLs analysed in this paper are chosen from those used and designed to synchronize to the grid signal, which can work with unknown values of the input signal frequency.

In general, the PLLs are constituted by three blocks. The phase detector (first block) provides a frequency error signal which is filtered by the loop filter (second block), whose output returns to the phase detector through the controlled oscillator (third block). The output of this last block is compared to the input signal within the phase detector block.

The way of implementing the phase detector causes the different technologies present in the technical literature as the Synchronous Reference Frame (SRF-PLL), [5], the Second-Order Generalized Integrator (SOGI-PLL), [7], [10], or the Enhanced PLL (EPLL), [11], [12], among others.

SRF-PLL is the most used in applications involving power electronics and power systems due to its simple implementation. It is based on creating a quadrature signal by delaying the original single-phase signal by one-fourth of the grid fundamental period, [13]. To create the quadrature signal there are a great variety of methods [14], [15, p.].

EPLL is also very popular in single-phase applications. Unlike the rest of PLLs presented and as an improvement in relation to the phase detection block, it uses an adaptative notch filter. However, a great disadvantage with respect to other PLLs is that it does not present disturbance rejection in every working conditions [16]. From any input signal, EPLL provides its fundamental component, amplitude, frequency and phase, [11].

PLL methods based on the second order generalized integrator (SOGI) are also very popular. Their main characteristics are robust performance, good disturbance rejection and fast transient response [17], at the expense of greater complexity in terms of architecture [14], [18], [19]. One of the most popular is SOGI-based frequency-locked loop (SOGI-FLL) [20], due to its good results when non conformities as sag, swell or imbalance, are present in the grid voltage [21].

The vast majority of PLL techniques present in the literature are constituted by a series of elements that have to be tuned to the input signal parameters. These elements are mainly fix or adaptive filters in the phase detector block [22]-[24], and loop filter in the controlled oscillator. As a consequence of increasing the complexity of the architecture, the PLL blocking time and the computation time will also increase.

III. RESULTS OF APPLYING THE CONSIDERED PLL TO THE GRID SYNCHRONIZATION.

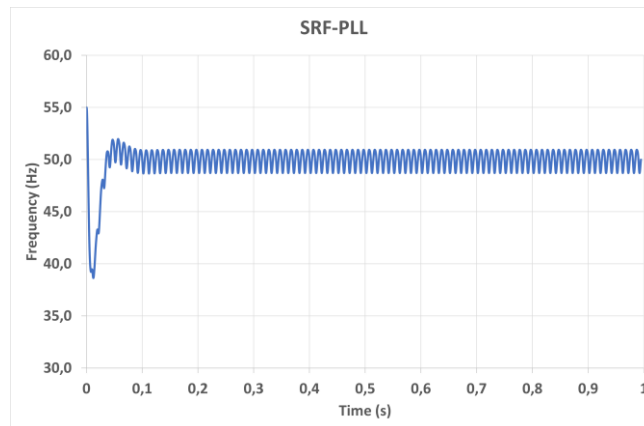
In this section, the PLL presented in section II are applied to the synchronization to the grid voltage. To do that, a distorted 50 Hz input signal has been chosen. The input signal expression for $n=9$ (harmonic number), is shown in equation (1). $inp_sig = V \sin[\omega u + \varphi] + V \sin[\omega u + \varphi] + \dots + V \sin[\omega u + \varphi]$ (1)

where: V: amplitude (V).

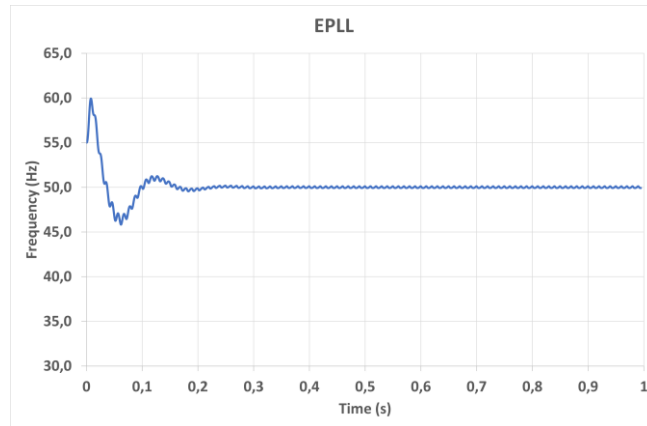
ω : angular velocity (rad/s).

φ : phase (rad). u: time (s).

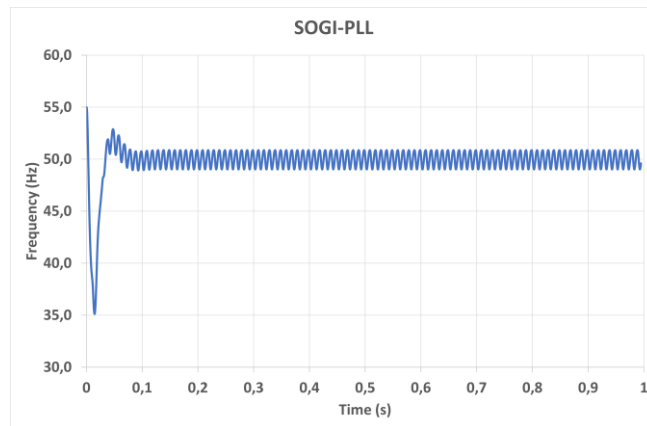
Figure 1 presents the results of using SRF-PLL, EPLL and SOGI-PLL, respectively, to track the distorted input signal expressed in equation (1), with the same frequency as the grid voltage (50 Hz). This figure shows the frequency provided by each one. All of them track the input signal frequency correctly. In addition, EPLL and SOGI-PLL provide the fundamental component of the input signal. The results obtained when they are applied to the highly distorted input signal expressed in equation (1), are presented in figure 2. As can be seen these two PLLs present disturbance rejection.



a. SRF-PLL

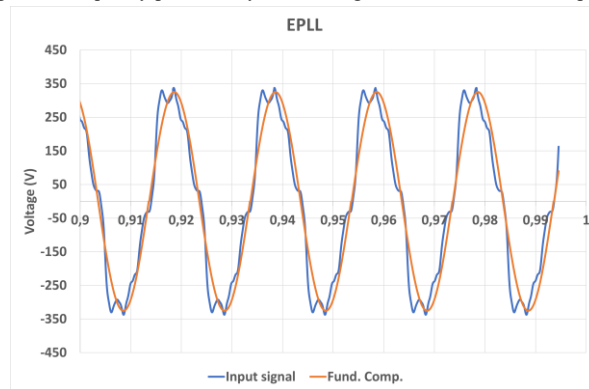


b. EPLL

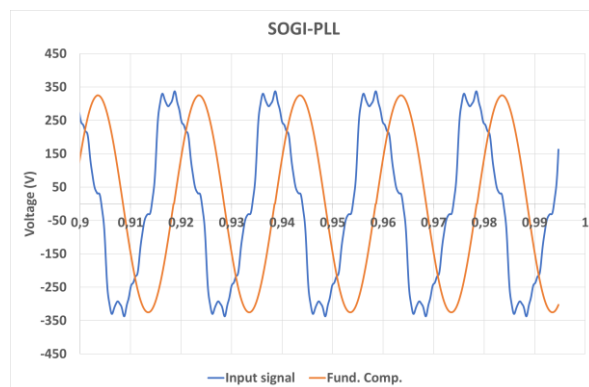


c. SOGI-PLL

Figure 1. Frequency provided by the PLL algorithms with a distorted input signal.



a. EPLL



b. SOGI-PLL

Figure 2. Fundamental component provided by the PLL algorithms with a distorted input signal.

IV. RESULTS OBTAINED IN DIFFERENT APPLICATIONS.

In this section, the PLL described in section II are applied to an application different from the synchronization to the grid voltage. The application chosen in this paper has been the modulated frequency, MF, into the communications framework.

Below are shown different figures with the results of applying those three PLLs in the range of MF. Specifically, they have been applied to an input signal which is the result of modulate the baseband signal whose angular velocity is presented in equation (2) by means of a carrier signal with the angular velocity presented in equation (3). Equation (4) presents the expression of the modulated signal. The range of MF frequency is 87.5 – 108 MHz.

$$\begin{aligned} \omega_b &= 2\pi 2000 \quad (2) \quad \omega_c = 2\pi 90E6 \quad (3) \\ \text{inp_sig} &= \cos \left[\omega_c \cdot u + m \left(\frac{1000\sqrt{2}}{\omega_b} \sin(\omega_b \cdot u) \right) \right] \quad (4) \end{aligned}$$

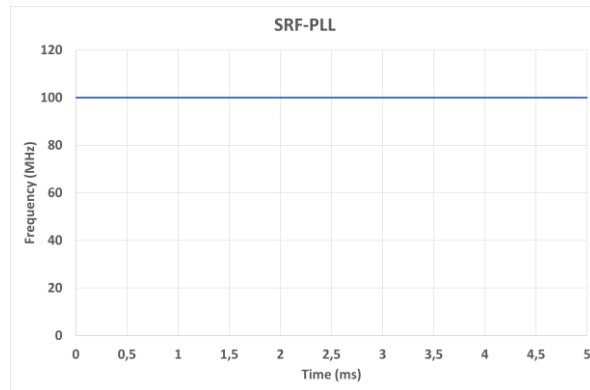
where:

ω_b : angular velocity of the baseband signal, to be modulated (rad/s). ω_c : angular velocity of the carrier signal (rad/s). m : modulating index with a value of 15000 in this case.
 u : time (s)

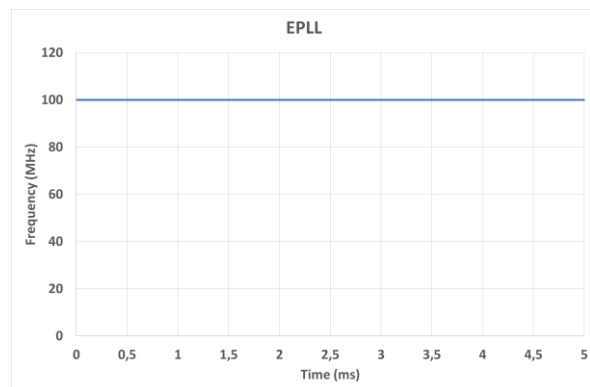
A. Results obtained when PLLs are applied to MF without tuning.

In this subsection, SRF-PLL, EPLL and SOGI-PLL are applied to the modulated signal whose expression is presented in equations (2) to (4). Filters and controllers included in the PLLs are tuned for the 50 Hz corresponding to the grid synchronization (applications for which they were designed).

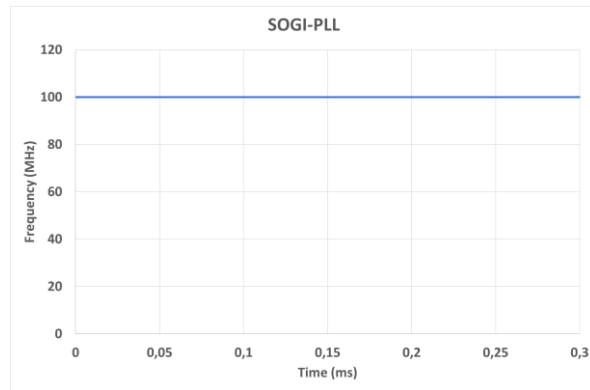
Figure 3 presents the frequency obtained applying SRFPLL, EPLL and SOGI-PLL, respectively, to the modulated signal indicated in equation (4). As can be seen, they are not able to track the signal. They don't even flinch. To make appreciable this fact, the initial frequency has been set at 100 MHz to initialise the three PLLs. In this way, their performance can be better assessed.



a) SRF-PLL



b) EPLL



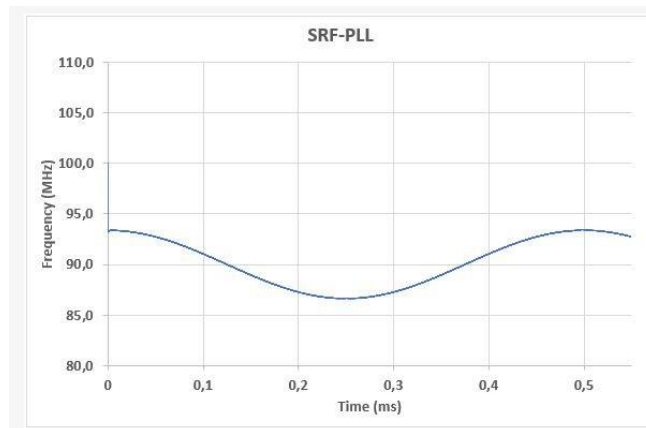
c) SOGI-PLL

Figure 3. Frequency provided by the PLLs when are applied to a modulated signal without adjusting filters parameters. a) SRF-PLL, b) EPLL, c) SOGI-PLL

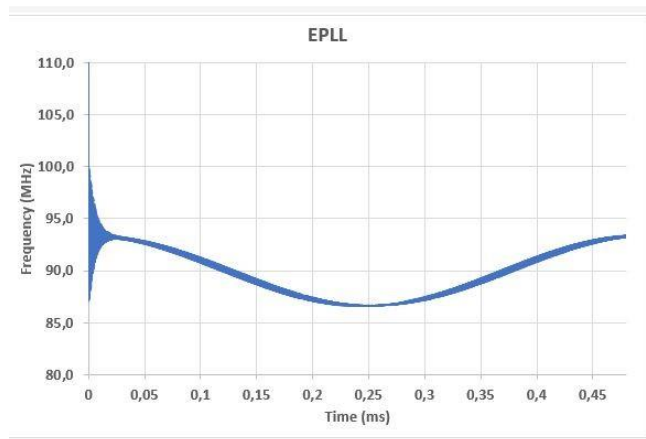
These results were predictable because the internal filters and controllers involved in the PLLs had not been tuned to the conditions presented by the new input signal.

B. Results obtained when PLLs are applied to MF with the necessary tuning.

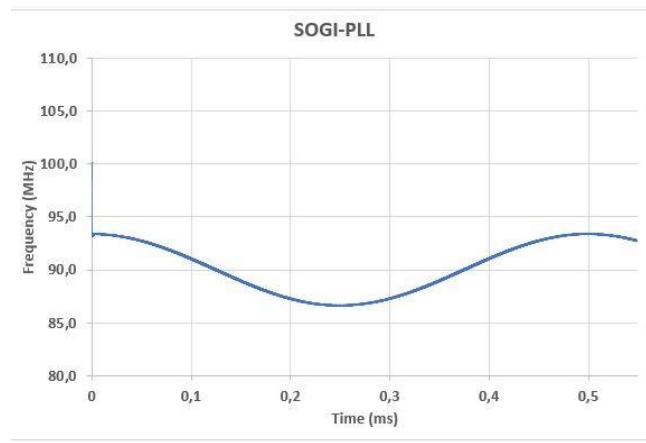
In view of the results obtained in the previous subsection, in this section those same PLLs are applied to the same input signal, but after performing the necessary tuning of the filters and controllers.



a) SRF-PLL



b) EPLL



c) SOGI-PLL

Figure 4. Frequency obtained applying the PLLs to a modulated signal adjusting filters parameters. a) SRF-PLL, b) EPLL, c) SOGI-PLL

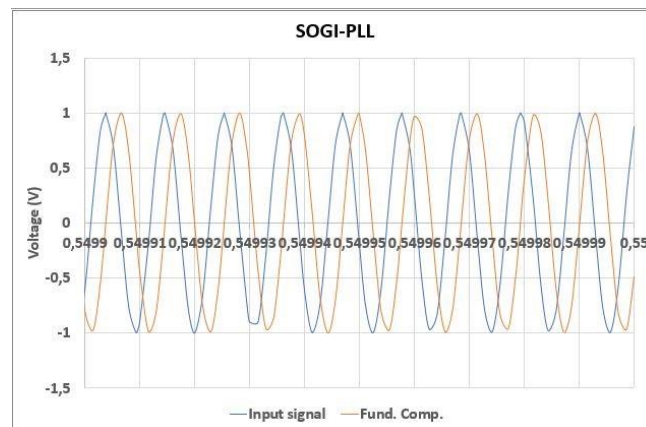


Figure 5. Fundamental component provided by the SOGI-PLL versus the input signal, which is frequency modulated, adjusting filters' parameters.

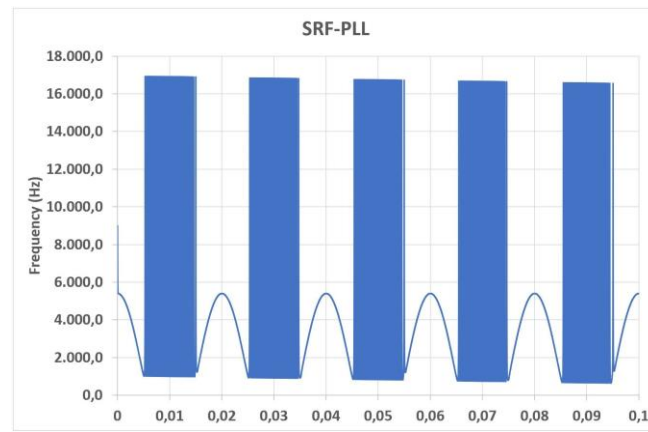
The frequency obtained is presented in figure 4. It shows that the three PLLs are able to track the input signal frequency. Figure 5 shows the fundamental component provided by the SOGI-PLL. It can be observed the optimum tracking achieved by the considered PLLs with the adjustment of their parameters.

C. Results obtained when PLLs are applied to MF tuning for an initial frequency different from the actual.

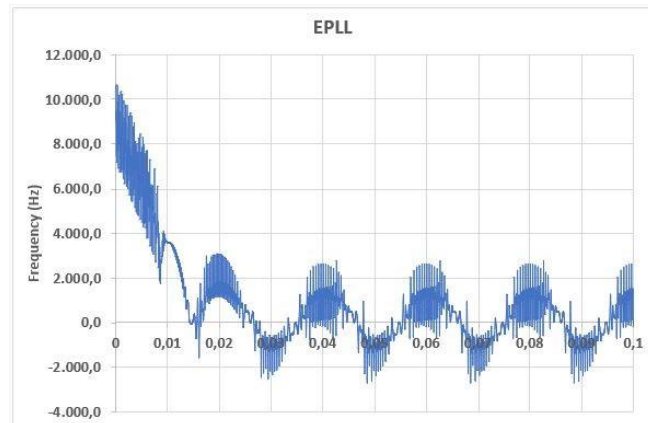
Results obtained in subsection B can't be extrapolated to any conditions. Effectively, the considered PLLs provide good results when they are tuned for the input signal parameters. However, in some applications, the frequency is unknown, and they must be tuned to the estimated frequency, which can be the actual or not. To analyse the PLLs behaviour in this case, the next case has been designed:

- The application is the MF again. Thus, the input signal is the expressed in equation (4).
- Base frequency is 50 Hz
- Carrier frequency is 900 Hz.
- The PLLs have been tuned to an initial estimated value of 9 kHz.

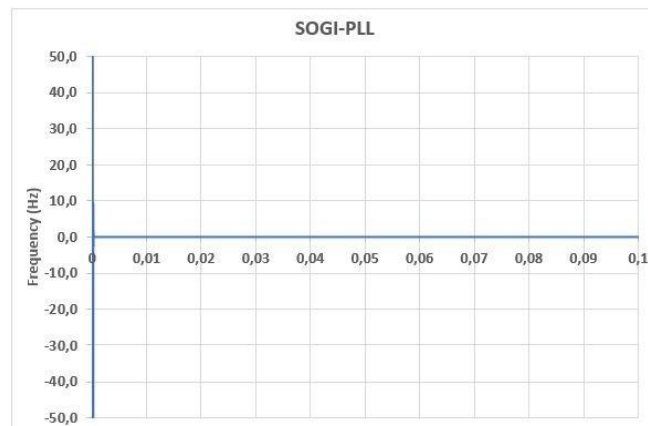
The results are presented in figure 6. As can be seen, now, the PLLs try to follow the input signal, although the results are not good. None of them achieve to track the input signal frequency.



a) SRF-PLL



b) EPLL



c) SOGI-PLL

Figure 6. Frequency obtained applying the PLLs to a modulated signal (50 Hz) with a 900 Hz adjusting the parameters to an initial value of 9 kHz

To clarify the results provided by each considered PLL circuit, a summary is presented in Table I.

TABLE I PLL COMPARATIVE

	SRF-PLL	EPLL	SOGI-PLL
It tracks the input signal phase and frequency after being tuned in.	x	x	x
It is not affected by the input signal distortion in any work conditions.	x		x
It is simple and has low computational cost.	x	x	
It provides the input signal fundamental component waveform.		x	x
It follows the phase and frequency of the input signal without being tuned each time.			

V. CONCLUSIONS

In this paper, the most used PLL circuits to synchronize to the grid waveforms, able to work with an unknown initial value of the frequency, have been chosen from the technical literature. Their performance has been studied in the monitoring of input signals with conditions different from those presented by the grid voltage, in synchronization. These different conditions are those that occur, for example, in communications applications. The results obtained, prove that the assessed PLLs present a good behaviour if the filters and controlled involved in them are tuned to the input signal frequency. In this case, the PLLs provide a signal which tracks the input signal frequency. It could be thought they are universal PLL. However, if the value of the frequency is unknown, the tuning has to be carried out to an estimated frequency, different from the actual one. The results obtained in this paper prove that, in these new conditions, the assessed PLLs do not achieve to track the input signal frequency. Thus, the PLLs analyzed in this paper and carefully chosen are not able to carry out frequency sweeps. Therefore, any of them can be considered as the universal PLL.

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